



# Op Amp Applications Handbook



Analog Devices, Inc.

By Walt Jung



# ***Op Amp Applications Handbook***

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# *Op Amp Applications Handbook*



*Walt Jung, Editor*  
*with the technical staff of Analog Devices*

A Volume in the Analog Devices Series



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# Foreword

The signal-processing products of Analog Devices, Inc. (ADI), along with those of its worthy competitors, have always had broad applications, but in a special way: they tend to be used in critical roles making possible—and at the same time limiting—the excellence in performance of the device, instrument, apparatus, or system using them.

Think about the *op amp*—how it can play a salient role in amplifying an ultrasound wave from deep within a human body, or measure and help reduce the error of a feedback system; the *data converter*—and its critical position in translating rapidly and accurately between the world of tangible physics and the world of abstract digits; the *digital signal processor*—manipulating the transformed digital data to extract information, provide answers, and make crucial instant-by-instant decisions in control systems; *transducers*, such as the life-saving MEMS accelerometers and gyroscopes; and even *control chips*, such as the one that empowers the humble thermometric junction placed deep in the heart of a high-performance—but very vulnerable—microcomputer chip.

From its founding two human generations ago, in 1965, ADI has been committed to a leadership role in designing and manufacturing products that meet the needs of the existing market, anticipate the near-term needs of present and future users, and envision the needs of users yet unknown—and perhaps *unborn*—who will create the markets of the future. These existing, anticipated and envisioned “needs” must perforce include far more than just the design, manufacture and timely delivery of a physical device that performs a function reliably to a set of specifications at a competitive price.

We’ve always called a product that satisfies these needs “the augmented product,” but what does this mean?

The *physical* product is a highly technological product that, above all, requires *knowledge* of its possibilities, limitations and subtleties. But when the earliest generations—and to some extent later generations—of such a product appear in the marketplace, there exist few (if any) school courses that have produced graduates proficient in its use. There are few knowledgeable designers who can foresee its possibilities. So we have the huge task of creating awareness; teaching about principles, performance measures, and existing applications; and providing ideas to stimulate the imagination of those creative users who will provide our next round of challenges.

This problem is met by deploying people and publications. The *people* are Applications Engineers, who can deal with user questions arriving via phone, fax, and e-mail—as well as working with users in the field to solve particular problems. These experts also spread the word by giving seminars to small and large groups for purposes from inspiring the creative user to imbuing the system, design, and components engineer with the nuts-and-bolts of practice. The *publications*—both in hard copy and on-line—range from authoritative handbooks, such as the present volume, comprehensive data sheets, application notes, hardware and software manuals, to periodic publications, such as “Solutions Bulletins” and our unique *Analog Dialogue*—the sole survivor among its early peers—currently in its 38<sup>th</sup> year of continuous publication in print and its 6<sup>th</sup> year of regular publication on the Internet.

This book is the ultimate expression of product “augmentation” as it relates to operational amplifiers. In some senses, it can be considered a descendant of two early publications. The first is a 1965 set of *Op Amp*



*Notes* (Parts 1, 2, 3, and 4), written by Analog Devices co-founder Ray Stata, with the current text directly reflecting these roots. Much less directly would be the 1974 first edition of the *IC Op Amp Cookbook*, by Walter Jung. Although useful earlier books had been published by Burr-Brown, and by Dan Sheingold at Philbrick, these two timely publications were seminal in the early days of the silicon era, advocating the understanding and use of IC op amps to a market in the process of growing explosively. Finally, and perhaps more important to current students of the op amp art, would be the countless contributions of ADI design and applications engineers, amassed over the years and so highly evident within this new book.

Operational amplifiers have been marketed since 1953, and practical IC op amps have been available since the late 1960s. Yet, half a century later, there is still a need for a book that embraces the many aspects of op amp technology—one that is thorough in its technical content, that looks forward to tomorrow’s uses and back to the principles and applications that still make op amps a practical necessity today. We believe that this is such a book, and we commend Walter Jung for “augmenting” the op amp in such an interesting and accessible form.

*Ray Stata*

*Daniel Sheingold*

Norwood, Massachusetts, April 28, 2004

# Preface

**Op Amp Applications Handbook** is another book on the operational amplifier, or *op amp*. As the name implies, it covers the application of op amps, but does so on a broader scope. Thus it would be incorrect to assume that this book is simply a large collection of app notes on various devices, as it is far more than that. Any IC manufacturer in existence since the 1960s has ample application data on which to draw. In this case, however, Analog Devices, Inc. has had the benefit of applications material with a history that goes back beyond early IC developments to the preceding period of solid-state amplifiers in modular form, with links to the even earlier era of vacuum tube op amps and analog computers, where the operational amplifier began.

This book brings some new perspectives to op amp applications. It adds insight into op amp origins and historical developments not available elsewhere. Within its major chapters it also offers fundamental discussions of basic op amp operation; the roles of various device types (including both op amps and other specialty amplifiers, such as instrumentation amplifiers); the procedures for optimal interfacing to other system components such as ADCs and DACs, signal conditioning and filtering in data processing systems, and a wide variety of signal amplifiers. The book concludes with practical discussions of various hardware issues, such as passive component selection, printed circuit design, modeling and breadboarding, etc. In short, while this book does indeed cover op amp applications, it also covers a host of closely related design topics, making it a formidable toolkit for the analog designer.

The book is divided into 8 major chapters, and occupies nearly 1000 pages, including index. The chapters are outlined as follows:

Chapter 1, *Op Amp Basics*, has five sections authored by James Bryant, Walt Jung, and Walt Kester. This chapter provides fundamental op amp operating information. An introductory section addresses their ideal and non-ideal characteristics along with basic feedback theory. It then spans op amp device topologies, including voltage and current feedback models, op amp internal structures such as input and/or output architectures, the use of bipolar and/or FET devices, single supply/dual supply considerations, and op amp device specifications that apply to all types. The two final sections of this chapter deal with the operating characteristics of precision and high-speed op amp types. This chapter, itself a book-within-a-book, occupies about 118 pages.

Chapter 2, *Specialty Amplifiers*, has three sections authored by Walt Kester, Walt Jung, and James Bryant. This chapter provides information on those commonly used amplifier types that use op amp-like principles, but aren't op amps themselves—instead they are specialty amplifiers. The first section covers the design and application of differential input, single-ended output amplifiers, known as instrumentation amplifiers. The second section is on programmable gain amplifiers, which are op amp or instrumentation amplifier stages, designed to be dynamically addressable for gain. The final section of the chapter is on isolation amplifiers, which provide galvanic isolation between sections of a system. This chapter occupies about 52 pages.

Chapter 3, *Using Op Amps with Data Converters*, has five sections authored by Walt Kester, James Bryant, and Paul Hendriks. The first section is an introductory one, introducing converter terms and the concept of minimizing conversion degradation within the design of an op amp interface. The second section covers ADC and DAC specifications, including such critically important concepts as linearity, monotonicity,

missing codes. The third section covers driving ADC inputs in both single-ended and differential signal modes, op amp stability and settling time issues, level shifting, etc. This section also includes a discussion of dedicated differential driver amplifier ICs, as well as op amp-based ADC drivers. The fourth section is concerned with driving converter reference inputs, and optimal use of sources. The fifth and final section covers DAC output buffer amplifiers, using both standard op amp circuits as well as differential driver ICs. This chapter occupies about 54 pages.

Chapter 4, *Sensor Signal Conditioning*, has five sections authored by Walt Kester, James Bryant, Walt Jung, Scott Wurcer, and Chuck Kitchin. After an introductory section on sensor types and their processing requirements, the remaining four sections deal with the different sensor types. The second section is on bridge circuits, covering the considerations in optimizing performance with respect to bridge drive mode, output mode, and impedance. The third section covers strain, force, pressure, and flow measurements, along with examples of high performance circuits with representative transducers. The fourth section, on high impedance sensors, covers a multitude of measurement types. Among these are photodiode amplifiers, charge amplifiers, and pH amplifiers. The fifth section of the chapter covers temperature sensors of various types, such as thermocouples, RTDs, thermistor and semiconductor-based transducers. This chapter occupies about 82 pages.

Chapter 5, *Analog Filters*, has eight sections authored by Hank Zumbahlen. This chapter could be considered a stand-alone treatise on how to implement modern analog filters. The eight sections, starting with an introduction, include transfer functions, time domain response, standard responses, frequency transformations, filter realizations, practical problems, and design examples. This chapter is more mathematical than any other within the book, with many response tables as design aids. One key highlight is the design example section, where an online filter-builder design tool is described in active filter implementation examples using Sallen-Key, multiple feedback, state variable, and frequency dependent negative resistance filter types. This chapter, another book-within-a-book, occupies about 114 pages.

Chapter 6, *Signal Amplifiers*, has six sections authored by Walt Jung and Walt Kester. These sections are audio amplifiers, buffer amplifiers/driving capacitive loads, video amplifiers, communication amplifiers, amplifier ideas, and composite amplifiers. In the audio, video, and communications amplifier sections, various op amp circuit examples are shown, with emphasis in these sections on performance to high specifications— audio, video, or communications, as the case may be. The “amplifier ideas” section is a broad-range collection of various amplifier applications, selected for emphasis on creativity and innovation. The final section, on composite amplifiers, shows how additional discrete devices can be added to either the input or output of an op amp to enhance net performance. This book-within-a-book chapter occupies about 184 pages.

Chapter 7, *Hardware and Housekeeping Techniques*, has seven sections authored by Walt Kester, James Bryant, Walt Jung, Joe Buxton, and Wes Freeman. These sections are passive components, PCB design issues, op amp power supply systems, op amp input and output protection, thermal considerations, EMI/RFI considerations, and the final section, simulation, breadboarding and prototyping. All of these practical topics have a commonality that they are not completely covered (if at all) by the op amp data sheet. But, most importantly, they can be just as critical as the device specifications towards achieving the final results. This book-within-a-book chapter occupies about 158 pages.

Chapter 8, the *History* chapter has four sections authored by Walt Jung. It provides a detailed account of not only the beginnings of operational amplifiers, but also their progress and the ultimate evolution into the IC form known today. This began with the underlying development of feedback amplifier principles, by Harold Black and others at Bell Telephone Laboratories. From the first practical analog computer feedback amplifier building blocks used during World War II, vacuum tube op amps later grew in sophistication, popularity

and diversity of use. The first solid-state op amps were “black-brick” plug in modules, which in turn were followed by hybrid IC forms, using chip semiconductors on ceramic substrates. The first monolithic IC op amp appeared in the early 1960s, and there have been continuous developments in circuitry, processes and packaging since then. This chapter occupies about 68 pages, and includes several hundred literature references.

The book is concluded with a thorough index with three pointer types: subject, ADI part number, and standard part numbers.

## ***Acknowledgments***

A book on a scale such as **Op Amp Applications Handbook** isn’t possible without the work of many individuals. In the preparation phase many key contributions were made, and these are here acknowledged with sincere thanks. Of course, the first “Thank you” goes to ADI management, for project encouragement and support.

Hearty thanks goes next to Walt Kester of the ADI Central Applications Department, who freely offered his wisdom and counsel from many years of past ADI seminar publications. He also commented helpfully on the manuscript throughout. Special thanks go to Walt, as well as the many other named section authors who contributed material.

Thanks go also to the ADI Field Applications and Central Applications Engineers, who helped with comments and criticism. Ed Grokulsy, Bruce Hohman, Bob Marwin and Arnold Williams offered many helpful comments, and former ADI Applications Engineer Wes Freeman critiqued most of the manuscript, providing valuable feedback.

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Thanks to Carolyn Hobson, who was instrumental in obtaining many of the historical references.

Thanks to Judith Douville for preparation of the index and helpful manuscript comments.

Walt Jung and Walt Kester together prepared slides for the book, and coordinated the stylistic design. Walt Jung did the original book page layout and typesetting.

## ***Specific-to-Section Acknowledgments***

Acknowledged here are focused comments from many individuals, specific to the section cited. All were very much appreciated.

### **Op Amp History; Introduction:**

Particularly useful to this section of the project was reference information received from vacuum tube historian Gary Longrie. He provided information on early vacuum tube amplifiers, the feedback experiments of B. D. H. Tellegen at N. V. Philips, and made numerous improvement comments on the manuscript.

Mike Hummel provided the reference to Alan Blumlein’s patent of a negative feedback amplifier.

Dan Sheingold provided constructive comments on the manuscript.

Bob Milne offered many comments towards improvement of the manuscript.

### **Op Amp History; Vacuum Tube Op Amps:**

Particularly useful were numerous references on differential amplifiers, received from vacuum tube historian Gary Longrie. Gary also reviewed the manuscript and made numerous improvement comments. Without his enthusiastic inputs, the vacuum tube related sections of this narrative would be less complete.

Dan Sheingold supplied reference material, reviewed the manuscript, and made numerous constructive comments. Without his inputs, the vacuum tube op amp story would have less meaning.

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Bob Milne reviewed the manuscript and offered various improvement comments.

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### **Op Amp History; Solid-State Modular and Hybrid Op Amps:**

Particularly useful was information from two GAP/R alumni, Dan Sheingold and Bob Pease. Both offered many details on the early days of working with George Philbrick, and Bob Pease furnished a previously unpublished circuit of the P65 amplifier.

Dick Burwen offered detailed information on some of his early ADI designs, and made helpful comments on the development of the narrative.

Steve Guinta and Charlie Scouten provided many of the early modular op amp schematics from the ADI Central Applications Department archival collection.

Lew Counts assisted with comments on the background of the high speed modular FET amplifier developments.

Walt Kester provided details on the HOS-050 amplifier and its development as a hybrid IC product at Computer Labs.

### **Op Amp History; IC Op Amps:**

Many helpful comments on this section were received, and all are very much appreciated. In this regard, thanks go to Derek Bowers, JoAnn Close, Lew Counts, George Erdi, Bruce Hohman, Dave Kress, Bob Marwin, Bob Milne, Reza Moghimi, Steve Parks, Dan Sheingold, Scott Wurcer, and Jerry Zis

### **Op Amp Basics; Introduction:**

Portions of this section were adapted from Ray Stata's "Operational Amplifiers - Part I," **Electromechanical Design**, September, 1965.

Bob Marwin, Dan Sheingold, Ray Stata, and Scott Wayne contributed helpful comments.

### **Op Amp Basics; Structures:**

Helpful comments on various op amp schematics were received from ADI op amp designers Derek Bowers, Jim Butler, JoAnn Close, and Scott Wurcer.

### **Signal Amplifiers; Audio Amplifiers:**

Portions of this section were adapted from Walt Jung, “Audio Preamplifiers, Line Drivers, and Line Receivers,” Chapter 8 of Walt Kester, **System Application Guide**, Analog Devices, Inc., 1993, ISBN 0-916550-13-3, pp. 8-1 to 8-100.

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### **Signal Amplifiers; Amplifier Ideas:**

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### **Signal Amplifiers, Composite Amplifiers:**

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### **Hardware and Housekeeping Techniques; Passive Components and PCB Design Issues:**

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### **Hardware and Housekeeping Techniques; EMI/RFI Considerations:**

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*The above acknowledgments document helpful inputs received for the Analog Devices 2002 Amplifier Seminar edition of **Op Amp Applications**. In addition, Scott Wayne and Claire Shaw aided in preparation of the manuscript for this Newnes edition.*

While reasonable efforts have been made to make this work error-free, some inaccuracies may have escaped detection. The editors accept responsibility for error correction within future editions, and will appreciate errata notification(s).

*Walt Jung, Editor  
**Op Amp Applications Handbook**  
May 14, 2004*

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# Op Amp History Highlights

**1928**

Harold S. Black applies for patent on his feedback amplifier invention.

**1930**

Harry Nyquist applies for patent on his regenerative amplifier (patent issued in 1933).

**1937**

U.S. Patent No. 2,102,671 issued to H.S. Black for "Wave Translation System."

B.D.H. Tellegen publishes a paper on feedback amplifiers, with attributions to H.S. Black and K. Posthumus.

Hendrick Bode files for an amplifier patent, issued in 1938.

**1941**

Stewart Miller publishes an article with techniques for high and stable gain with response to dc, introducing "cathode compensation."

Testing of prototype gun director system called the T10 using feedback amplifiers. This later leads to the M9, a weapon system instrumental in winning WWII.

Patent filed by Karl D. Swartzel Jr. of Bell Labs for a "Summing Amplifier," with a design that could well be the genesis of op amps. Patent not issued until 1946.

**1946**

George Philbrick founds company, George A. Philbrick Researches, Inc. (GAP/R). His work was instrumental in op amp development.

**1947**

Medal for Merit award given to Bell Labs's M9 designers Lovell, Parkinson, and Kuhn. Other contributors to this effort include Bode and Shannon.

Operational amplifiers first referred to by name in Ragazzini's key paper "Analysis of Problems in Dynamics by Electronic Circuits." It references the Bell Labs work on what became the M9 gun director, specifically referencing the op amp circuits used.

Bardeen, Brattain, and Shockley of Bell Labs discover the transistor effect.

**1948**

George A. Philbrick publishes article describing a single-tube circuit that performs some op amp functions.

**1949**

Edwin A. Goldberg invents chopper-stabilized vacuum tube op amp.

**1952**

Granino and Theresa Korn publish textbook *Electronic Analog Computers*, which becomes a classic work on the uses and methodology of analog computing, with vacuum tube op amp circuits.

**1953**

First commercially available vacuum tube op amp introduced by GAP/R.

**1954**

Gordon Teal of Texas Instruments develops a silicon transistor.

**1956**

GAP/R publishes manual for K2-W and related amplifiers, that becomes a seminal reference.

Nobel Prize in Physics awarded to Bardeen, Brattain, and Shockley of Bell Labs for the transistor.

Burr-Brown Research Corporation formed. It becomes an early modular solid-state op amp supplier.



**1958**

Jack Kilby of Texas Instruments invents the integrated circuit (IC).

**1959**

Jean A. Hoerni files for a patent on the planar process, a means of stabilizing and protecting semiconductors.

**1962**

George Philbrick introduces the PP65, a square outline, 7-pin modular op amp which becomes a standard and allows the op amp to be treated as a *component*.

**1963**

Bob Widlar of Fairchild designs the  $\mu$ A702, the first generally recognized monolithic IC op amp.

**1965**

Fairchild introduces the milestone  $\mu$ A709 IC op amp, also designed by Bob Widlar.

Analog Devices, Inc. (ADI) is founded by Matt Lorber and Ray Stata. Op amps were their first product.

**1967**

National Semiconductor Corp. (NSC) introduces the LM101 IC op amp, also designed by Bob Widlar, who moved to NSC from Fairchild. This device begins a second generation of IC op amps.

*Analog Dialogue* magazine is first published by ADI.

**1968**

The  $\mu$ A741 op amp, designed by Dave Fullagar, is introduced by Fairchild and becomes the standard op amp.

**1969**

Dan Sheingold takes over as editor of *Analog Dialogue* (and remains so today).

**1970**

Model 45 high speed FET op amp introduced by ADI.

**1972**

Russell and Frederiksen of National Semiconductor Corp. introduce an amplifier technique that leads to the LM324, the low cost, industry-standard general-purpose quad op amp.

**1973**

Analog Devices introduces AD741, a high-precision 741-type op amp.

**1974**

Ion implantation, a new fabrication technique for making FET devices, is described in a paper by Rod Russell and David Culner of National Semiconductor.

**1988**

ADI introduces a high speed 36V CB process and a number of fast IC op amps. High performance op amps and op amps designed for various different categories continue to be announced throughout the 1980s and 1990s, and into the twenty-first century.

*Chapter 8 provides a detailed narrative of op amp history.*

## CHAPTER 1

# *Op Amp Basics*

- Section 1-1: Introduction
- Section 1-2: Op Amp Topologies
- Section 1-3: Op Amp Structures
- Section 1-4: Op Amp Specifications
- Section 1-5: Precision Op Amps
- Section 1-6: High Speed Op Amps

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# Op Amp Basics

*James Bryant, Walt Jung, Walt Kester*

Within Chapter 1, discussions are focused on the basic aspects of op amps. After a brief introductory section, this begins with the fundamental *topology* differences between the two broadest classes of op amps, those using *voltage feedback* and *current feedback*. These two amplifier types are distinguished more by the nature of their internal circuit topologies than anything else. The voltage feedback op amp topology is the classic structure, having been used since the earliest vacuum tube based op amps of the 1940s and 1950s, through the first IC versions of the 1960s, and includes most op amp models produced today. The more recent IC variation of the current feedback amplifier has come into popularity in the mid-to-late 1980s, when higher speed IC op amps were developed. Factors distinguishing these two op amp types are discussed at some length.

Details of op amp input and output *structures* are also covered in this chapter, with emphasis on how such factors potentially impact application performance. In some senses, it is logical to categorize op amp types into performance and/or application classes, a process that works to some degree, but not altogether.

In practice, once past those obvious application distinctions such as “high speed” versus “precision,” or “single” versus “dual supply,” neat categorization breaks down. This is simply the way the analog world works. There is much crossover between various classes, i.e., a high speed op amp can be either single or dual-supply, or it may even fit as a precision type. A low power op amp may be precision, but it need not necessarily be single-supply, and so on. Other distinction categories could include the input stage type, such as FET input (further divided into JFET or MOS, which, in turn, are further divided into NFET or PFET and PMOS and NMOS, respectively), or bipolar (further divided into NPN or PNP). Then, all of these categories could be further described in terms of the type of input (or output) stage used.

So, it should be obvious that categories of op amps are like an infinite set of analog gray scales; *they don't always fit neatly into pigeonholes, and we shouldn't expect them to*. Nevertheless, it is still very useful to appreciate many of the aspects of op amp design that go into the various structures, as these differences directly influence the optimum op amp choice for an application. Thus structure differences are application drivers, since we choose an op amp to suit the nature of the application—for example, single-supply.

In this chapter various op amp performance *specifications* are also discussed, along with those specification differences that occur between the broad distinctions of voltage or current feedback topologies, as well as the more detailed context of individual structures. Obviously, op amp specifications are also application drivers; in fact, they are the most important since they will determine system performance. We choose the best op amp to fit the application, based on the required bias current, bandwidth, distortion, and so forth.

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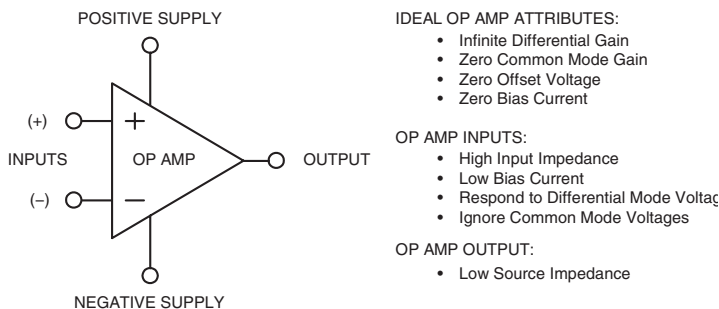
# Introduction

Walt Jung

As a precursor to more detailed sections following, this introductory chapter portion considers the most basic points of op amp operation. These initial discussions are oriented around the more fundamental levels of op amp applications. They include: *Ideal Op Amp Attributes*, *Standard Op Amp Feedback Hookups*, *The Non-Ideal Op Amp*, *Op Amp Common-Mode Dynamic Range(s)*, the various *Functionality Differences of Single and Dual-Supply Operation*, and the *Device Selection* process.

Before op amp applications can be developed, some requirements are in order. These include an understanding of how the fundamental op amp operating modes differ, and whether dual-supply or single-supply device functionality better suits the system under consideration. Given this, then device selection can begin and an application developed.

First, an *operational amplifier* (hereafter simply op amp) is a differential input, single-ended output amplifier, as shown symbolically in Figure 1-1. This device is an amplifier intended for use with *external feedback elements*, where these elements determine the resultant function, or *operation*. This gives rise to the name “operational amplifier,” denoting an amplifier that, by virtue of different feedback hookups, can perform a variety of operations.<sup>1</sup> At this point, note that there is no need for concern with any actual technology to implement the amplifier. Attention is focused more on the behavioral nature of this building block device.



**Figure 1-1: The ideal op amp and its attributes**

An op amp processes small, differential mode signals appearing between its two inputs, developing a single-ended output signal referred to a power supply common terminal. Summaries of the various ideal op amp attributes are given in Figure 1-1. While real op amps will depart from these ideal attributes, it is very helpful for first-level understanding of op amp behavior to consider these features. Further, although these initial discussions talk in idealistic terms, they are also flavored by pointed mention of typical “real world” specifications—for a beginning perspective.

<sup>1</sup> The actual *naming* of the operational amplifier occurred in the classic Ragazinni, et al paper of 1947 (see Reference 1). However, analog computations using op amps as we know them today began with the work of the Clarence Lovell-led group at Bell Labs, around 1940 (acknowledged generally in the Ragazinni paper).

It is also worth noting that this op amp is shown with five terminals, a number that happens to be a minimum for real devices. While some single op amps may have more than five terminals (to support such functions as frequency compensation, for example), none will ever have fewer. By contrast, those elusive ideal op amps don't require power, and symbolically function with just four pins.<sup>2</sup>

### ***Ideal Op Amp Attributes***

An ideal op amp has infinite gain for *differential* input signals. In practice, real devices will have quite high gain (also called *open-loop gain*) but this gain won't necessarily be precisely known. In terms of specifications, gain is measured in terms of  $V_{OUT}/V_{IN}$ , and is given in V/V, the dimensionless numeric gain. More often, however, gain is expressed in decibel terms (dB), which is mathematically  $\text{dB} = 20 \bullet \log(\text{numeric gain})$ . For example, a numeric gain of 1 million ( $10^6$  V/V) is equivalent to a 120 dB gain. Gains of 100 dB – 130 dB are common for precision op amps, while high speed devices may have gains in the 60 dB – 70 dB range.

Also, an ideal op amp has zero gain for signals *common* to both inputs, that is, *common-mode* (CM) signals. Or, stated in terms of the rejection for these common-mode signals, an ideal op amp has infinite *CM rejection* (CMR). In practice, real op amps can have CMR specifications of up to 130 dB for precision devices, or as low as 60 dB–70 dB for some high speed devices.

The ideal op amp also has zero *offset voltage* ( $V_{OS} = 0$ ), and draws zero *bias current* ( $I_B = 0$ ) at both inputs. Within real devices, actual offset voltages can be as low as 1  $\mu\text{V}$  or less, or as high as several mV. Bias currents can be as low as a few fA, or as high as several  $\mu\text{A}$ . This extremely wide range of specifications reflects the different input structures used within various devices, and is covered in more detail later in this chapter.

The attribute headings within Figure 1-1 for INPUTS and OUTPUT summarize the above concepts in more succinct terms. In practical terms, another important attribute is the concept of *low source impedance*, at the output. As will be seen later, low source impedance enables higher useful gain levels within circuits.

To summarize these idealized attributes for a signal processing amplifier, some of the traits might at first seem strange. However, it is critically important to reiterate that op amps simply are never intended for use without overall feedback. In fact, as noted, the connection of a suitable *external* feedback loop defines the *closed-loop* amplifier's gain and frequency response characteristics.

Note also that all real op amps have a positive and negative power supply terminal, but rarely (if ever) will they have a separate ground connection. In practice, the op amp output voltage becomes referred to a power supply common point. *Note: This key point is further clarified with the consideration of typically used op amp feedback networks.*

The basic op amp hookup of Figure 1-2 applies a signal to the (+) input, and a (generalized) network delivers a fraction of the output voltage to the (–) input terminal. This constitutes *feedback*, with the op amp operating in *closed-loop* fashion. The feedback network (shown here in general form) can be resistive or reactive, linear or nonlinear, or any combination of these. More detailed analysis will show that the circuit gain characteristic as a whole follows the inverse of the feedback network transfer function.

The concept of feedback is both an essential and salient point concerning op amp use. With feedback, the net closed-loop gain characteristics of a stage such as Figure 1-2 become primarily dependent upon a set of *external components* (usually passive). Thus behavior is less dependent upon the relatively unstable amplifier open-loop characteristics.

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<sup>2</sup> Such an op amp generates its own power, has two input pins, an output pin, and an output common pin.

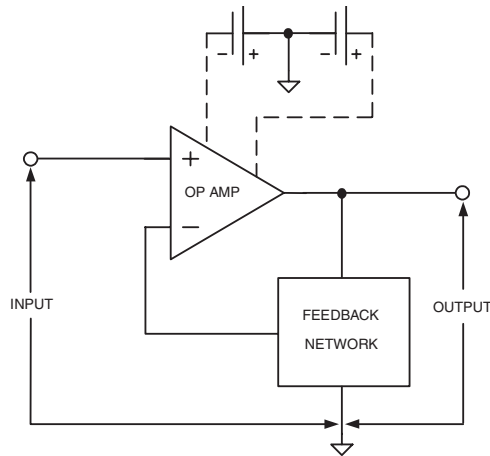


Figure 1-2: A generalized op amp circuit with feedback applied

Note that within Figure 1-2, the input signal is applied between the op amp (+) input and a *common* or *reference point*, as denoted by the ground symbol. It is important to note that this reference point is also common to the output and feedback network. By definition, the op amp stage's output signal appears between the output terminal/feedback network input, and this common ground. This single relevant fact answers the “Where is the op amp grounded?” question so often asked by those new to the craft. The answer is simply that it is grounded *indirectly*, by virtue of the commonality of its input, the feedback network, and the power supply, as is shown in Figure 1-2.

To emphasize how the input/output signals are referenced to the power supply, dual supply connections are shown dotted, with the  $\pm$  power supply midpoint common to the input/output signal ground. But do note, while all op amp application circuits may not show full details of the power supply connections, every *real* circuit will always use power supplies.

## Standard Op Amp Feedback Hookups

Virtually all op amp feedback connections can be categorized into just a few basic types. These include the two most often used, *noninverting* and *inverting* voltage gain stages, plus a related *differential* gain stage. Having discussed above just the attributes of the ideal op amp, at this point it is possible to conceptually build basic gain stages. Using the concepts of infinite gain, zero input offset voltage, zero bias current, and so forth, standard op amp feedback hookups can be devised. For brevity, a full mathematical development of these concepts isn't included here (but this follows in a subsequent section). The end-of-section references also include such developments.



## The Noninverting Op Amp Stage

The op amp noninverting gain stage, also known as a *voltage follower with gain*, or simply *voltage follower*, is shown in Figure 1-3.

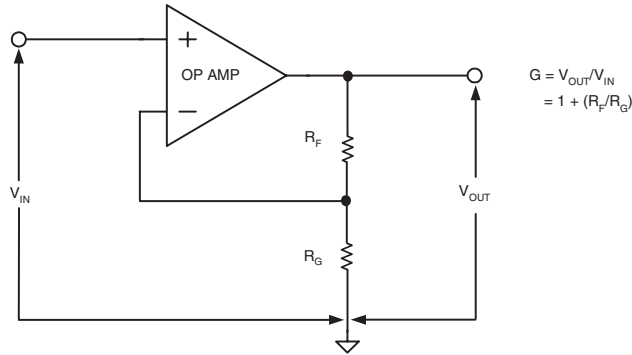


Figure 1-3: The noninverting op amp stage (voltage follower)

This op amp stage processes the input  $V_{IN}$  by a gain of  $G$ , so a generalized expression for gain is:

$$G = \frac{V_{OUT}}{V_{IN}} \quad \text{Eq. 1-1}$$

Feedback network resistances  $R_F$  and  $R_G$  set the stage gain of the follower. For an ideal op amp, the gain of this stage is:

$$G = \frac{R_F + R_G}{R_G} \quad \text{Eq. 1-2}$$

For clarity, these expressions are also included in the figure. Comparison of this figure and the more general Figure 1-2 shows  $R_F$  and  $R_G$  here as a simple feedback network, returning a fraction of  $V_{OUT}$  to the op amp (–) input. (*Note that some texts may show the more general symbols  $Z_F$  and  $Z_G$  for these feedback components—both are correct, depending upon the specific circumstances.*)

In fact, we can make some useful general points about the network  $R_F - R_G$ . We will define the transfer expression of the network as seen from the top of  $R_F$  to the output across  $R_G$  as  $\beta$ . Note that this usage is a general feedback network transfer term, *not* to be confused with bipolar transistor forward gain.  $\beta$  can be expressed mathematically as:

$$\beta = \frac{R_G}{R_F + R_G} \quad \text{Eq. 1-3}$$

So, the feedback network returns a fraction of  $V_{OUT}$  to the op amp (–) input. Considering the ideal principles of zero offset and infinite gain, this allows some deductions on gain to be made. The voltage at the (–) input is forced by the op amp's feedback action to be equal to that seen at the (+) input,  $V_{IN}$ . Given this relationship, it is relatively easy to work out the ideal gain of this stage, which in fact turns out to be simply the inverse of  $\beta$ . This is apparent from a comparison of Eqs. 1-2 and 1-3.

Thus an ideal noninverting op amp stage gain is simply equal to  $1/\beta$ , or:

$$G = \frac{1}{\beta} \quad \text{Eq. 1-4}$$

This noninverting gain configuration is one of the most useful of all op amp stages, for several reasons. Because  $V_{IN}$  sees the op amp's high impedance (+) input, it provides an ideal interface to the driving source. Gain can easily be adjusted over a wide range via  $R_F$  and  $R_G$ , with virtually no source interaction.

A key point is the interesting relationship concerning  $R_F$  and  $R_G$ . Note that to satisfy the conditions of Eq. 1-2, only their *ratio* is of concern. In practice this means that stable gain conditions can exist over a range of actual  $R_F - R_G$  values, so long as they provide the same ratio.

If  $R_F$  is taken to zero and  $R_G$  open, the stage gain becomes unity, and  $V_{OUT}$  is then exactly equal to  $V_{IN}$ . This special noninverting gain case is also called a *unity gain follower*, a stage commonly used for buffering a source.

Note that this op amp example shows only a simple resistive case of feedback. As mentioned, the feedback can also be reactive, i.e.,  $Z_F$ , to include capacitors and/or inductors. In all cases, however, it must include a dc path, if we are to assume the op amp is being biased by the feedback (which is usually the case).

To summarize some key points on op amp feedback stages, we paraphrase from Reference 2 the following statements, which will always be found useful:

*The summing point idiom is probably the most used phrase of the aspiring analog artificer, yet the least appreciated. In general, the inverting (–) input is called the summing point, while the noninverting (+) input is represented as the reference terminal. However, a vital concept is the fact that, within linear op amp applications, the inverting input (or summing point) assumes the same absolute potential as the noninverting input or reference (within the gain error of the amplifier). In short, the amplifier tries to servo its own summing point to the reference.*

## The Inverting Op Amp Stage

The op amp inverting gain stage, also known simply as the *inverter*, is shown in Figure 1-4. As can be noted by comparison of Figures 1-3 and 1-4, the inverter can be viewed as similar to a follower, but with a transposition of the input voltage  $V_{IN}$ . In the inverter, the signal is applied to  $R_G$  of the feedback network and the op amp (+) input is grounded.

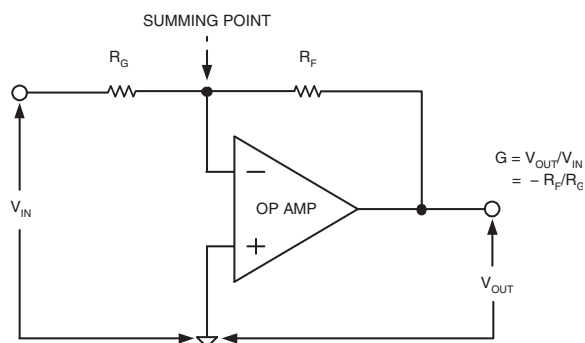


Figure 1-4: The inverting op amp stage (inverter)

The feedback network resistances  $R_F$  and  $R_G$  set the stage gain of the inverter. For an ideal op amp, the gain of this stage is:

$$G = -\frac{R_F}{R_G} \quad \text{Eq. 1-5}$$

For clarity, these expressions are again included in the figure. Note that a major difference between this stage and the noninverting counterpart is the input-to-output sign reversal, denoted by the minus sign in Eq. 1-5. Like the follower stage, applying ideal op amp principles and some basic algebra can derive the gain expression of Eq. 1-5.

The inverting configuration is also one of the more useful op amp stages. Unlike a noninverting stage, however, the inverter presents a relatively low impedance input for  $V_{IN}$ , i.e., the value of  $R_G$ . This factor provides a finite load to the source. While the stage gain can in theory be adjusted over a wide range via  $R_F$  and  $R_G$ , there is a practical limitation imposed at high gain, when  $R_G$  becomes relatively low. If  $R_F$  is zero, the gain becomes zero.  $R_F$  can also be made variable, in which case the gain is linearly variable over the dynamic range of the element used for  $R_F$ . As with the follower gain stage, the gain is ratio dependent, and is relatively insensitive to the exact  $R_F$  and  $R_G$  values.

The inverter's gain behavior, due to the principles of infinite op amp gain, zero input offset, and zero bias current, gives rise to an effective node of zero voltage at the  $(-)$  input. The input and feedback currents sum at this point, which logically results in the term *summing point*. It is also called a *virtual ground*, because of the fact it will be at the same potential as the grounded reference input.

Note that, technically speaking, *all* op amp feedback circuits have a summing point, whether they are inverters, followers, or a hybrid combination. The summing point is always the feedback junction at the  $(-)$  input node, as shown in Figure 1-4. However in follower type circuits this point isn't a virtual ground, since it follows the  $(+)$  input.

A special gain case for the inverter occurs when  $R_F = R_G$ , which is also called a *unity gain inverter*. This form of inverter is commonly used for generating complementary  $V_{OUT}$  signals, i.e.,  $V_{OUT} = -V_{IN}$ . In such cases it is usually desirable to match  $R_F$  to  $R_G$  accurately, which can readily be done by using a well-specified matched resistor pair.

A variation of the inverter is the *inverting summer*, a case similar to Figure 1-4, but with input resistors  $R_{G2}$ ,  $R_{G3}$ , etc (not shown). For a summer individual input resistors are connected to additional sources  $V_{IN2}$ ,  $V_{IN3}$ , and so forth, with their common node connected to the summing point. This configuration, called a *summing amplifier*, allows linear input current summation in  $R_F$ .<sup>3</sup>  $V_{OUT}$  is proportional to an inverse sum of input currents.

## The Differential Op Amp Stage

The op amp differential gain stage (also known as a *differential amplifier*, or *subtractor*) is shown in Figure 1-5.

Paired input and feedback network resistances set the gain of this stage. These resistors,  $R_F$ – $R_G$  and  $R'_F$ – $R'_G$ , *must be matched as noted*, for proper operation. Calculation of individual gains for inputs  $V_1$  and  $V_2$  and their linear combination derives the stage gain.

<sup>3</sup> The very first general-purpose op amp circuit is described by Karl Swartzel in Reference 3, and is titled "Summing Amplifier." This amplifier became a basic building block of the M9 gun director computer and fire control system used by Allied Forces in World War II. It also influenced many vacuum tube op amp designs that followed over the next two decades.

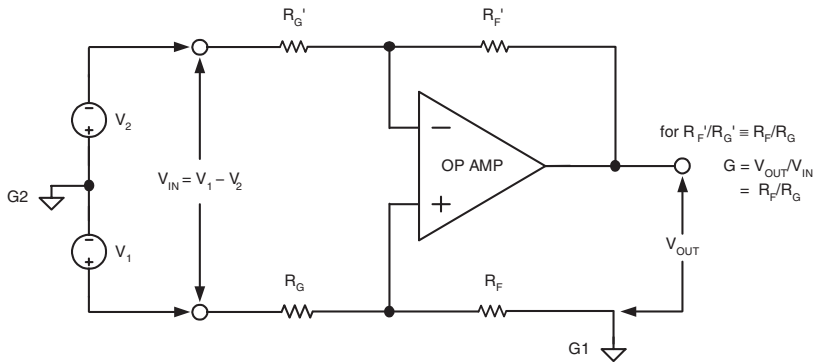


Figure 1-5: The differential amplifier stage (subtractor)

Note that the stage is intended to amplify the *difference* of voltages  $V_1$  and  $V_2$ , so the net input is  $V_{IN} = V_1 - V_2$ . The general gain expression is then:

$$G = \frac{V_{OUT}}{V_1 - V_2} \quad \text{Eq. 1-6}$$

For an ideal op amp and the resistor ratios matched as noted, the gain of this differential stage from  $V_{IN}$  to  $V_{OUT}$  is:

$$G = \frac{R_F}{R_G} \quad \text{Eq. 1-7}$$

The great fundamental utility that an op amp stage such as this allows is the property of rejecting voltages *common* to  $V_1 - V_2$ , i.e., common-mode (CM) voltages. For example, if noise voltages appear between grounds G1 and G2, the noise will be suppressed by the common-mode rejection (CMR) of the differential amp. The CMR however is only as good as the matching of the resistor ratios allows, so in practical terms it implies precisely trimmed resistor ratios are necessary. Another disadvantage of this stage is that the resistor networks load the  $V_1 - V_2$  sources, potentially leading to additional errors.

### The Nonideal Op Amp—Static Errors Due to Finite Amplifier Gain

One of the most distinguishing features of op amps is their staggering magnitude of dc voltage gain. Even the least expensive devices have typical voltage gains of 100,000 (100 dB), while the highest performance precision bipolar and chopper stabilized units can have gains as high 10,000,000 (140 dB), or more. Negative feedback applied around this much voltage gain readily accomplishes the virtues of closed-loop performance, making the circuit dependent only on the feedback components.

As noted above in the discussion of ideal op amp attributes, the behavioral assumptions follow from the fact that negative feedback, coupled with high open-loop gain, constrains the amplifier input error voltage (and consequently the error current) to infinitesimal values. The higher this gain, the more valid these assumptions become.

In reality, however, op amps *do* have finite gain and errors exist in practical circuits. The op amp gain stage of Figure 1-6 will be used to illustrate how these errors impact performance. In this circuit the op amp is ideal except for the finite open-loop dc voltage gain,  $A$ , which is usually stated as  $A_{VOL}$ .

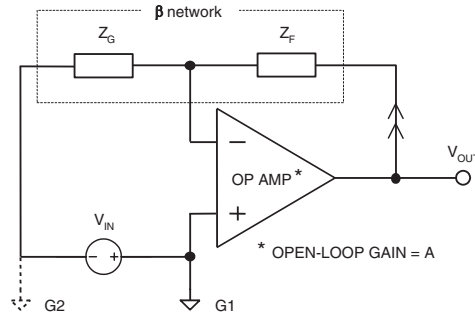


Figure 1-6: Nonideal op amp stage for gain error analysis

## Noise Gain (NG)

The first aid to analyzing op amps circuits is to differentiate between *noise gain* and *signal gain*. We have already discussed the differences between noninverting and inverting stages as to their signal gains, which are summarized in Eqs. 1-2 and 1-4, respectively. But, as can be noticed from Figure 1-6, the difference between an inverting and noninverting stage can be as simple as where the reference ground is placed. For a ground at point G1, the stage is an inverter; conversely, if the ground is placed at point G2 (with no G1) the stage is noninverting.

Note, however, that in terms of the feedback path, *there are no real differences*. To make things more general, the resistive feedback components previously shown are replaced here with the more general symbols  $Z_F$  and  $Z_G$ , otherwise they function as before. The feedback attenuation,  $\beta$ , is the same for both the inverting and noninverting stages:

$$\beta = \frac{Z_G}{Z_G + Z_F} \quad \text{Eq. 1-8}$$

Noise gain can now be simply defined as: *The inverse of the net feedback attenuation from the amplifier output to the feedback input*. In other words, the inverse of the  $\beta$  network transfer function. This can ultimately be extended to include frequency dependence (covered later in this chapter). Noise gain can be abbreviated as NG.

As noted, the inverse of  $\beta$  is the ideal noninverting op amp stage gain. Including the effects of finite op amp gain, a modified gain expression for the noninverting stage is:

$$G_{CL} = \frac{1}{\beta} \times \left[ \frac{1}{1 + \frac{1}{A_{VOL}\beta}} \right] \quad \text{Eq. 1-9}$$

where  $G_{CL}$  is the finite-gain stage's closed-loop gain, and  $A_{VOL}$  is the op amp open-loop voltage gain for loaded conditions.

It is important to note that this expression is identical to the ideal gain expression of Eq. 1-4, with the addition of the bracketed multiplier on the right side. Note also that this right-most term becomes closer and closer to unity, as  $A_{VOL}$  approaches infinity. Accordingly, it is known in some textbooks as the *error multiplier* term, when the expression is shown in this form.<sup>4</sup>

It may seem logical here to develop another finite gain error expression for an inverting amplifier, but in actuality there is no need. Both inverting and noninverting gain stages have a common feedback basis, which is the noise gain. So Eq. 1-9 will suffice for gain error analysis for both stages. Simply use the  $\beta$  factor as it applies to the specific case.

It is useful to note some assumptions associated with the rightmost error multiplier term of Eq. 1-9. For  $A_{VOL}\beta \gg 1$ , one assumption is:

$$\frac{1}{1 + \frac{1}{A_{VOL}\beta}} \approx 1 - \frac{1}{A_{VOL}\beta} \quad \text{Eq. 1-10}$$

This in turn leads to an estimation of the percentage error,  $\epsilon$ , due to finite gain  $A_{VOL}$ :

$$\epsilon(\%) \approx \frac{100}{A_{VOL}\beta} \quad \text{Eq. 1-11}$$

### Gain Stability

The closed-loop gain error predicted by these equations isn't in itself tremendously important, since the ratio  $Z_F/Z_G$  could always be adjusted to compensate for this error.

But note however that closed-loop gain *stability* is a very important consideration in most applications. Closed-loop gain instability is produced primarily by variations in open-loop gain due to changes in temperature, loading, and so forth.

$$\frac{\Delta G_{CL}}{G_{CL}} \approx \frac{\Delta A_{VOL}}{A_{VOL}} \times \frac{1}{A_{VOL}\beta} \quad \text{Eq. 1-12}$$

From Eq. 1-12, any variation in open-loop gain ( $\Delta A_{VOL}$ ) is reduced by the factor  $A_{VOL}\beta$ , insofar as the effect on closed-loop gain. This improvement in closed-loop gain stability is one of the important benefits of negative feedback.

### Loop Gain

The product  $A_{VOL}\beta$ , which occurs in the above equations, is called *loop gain*, a well-known term in feedback theory. The improvement in closed-loop performance due to negative feedback is, in nearly every case, proportional to loop gain.

The term "loop gain" comes from the method of measurement. This is done by breaking the closed feedback loop at the op amp output, and measuring the total gain around the loop. In Figure 1-6 for example, this could be done between the amplifier output and the feedback path (see arrows). To a first

<sup>4</sup> Some early discussions of this finite gain error appear in References 4 and 5. Terman uses the open-loop gain symbol of  $A$ , as we do today. West uses Harold Black's original notation of  $\mu$  for open-loop gain. The form of Eq. 1-9 is identical to Terman's (or to West's, substituting  $\mu$  for  $A$ ).

approximation, closed-loop output impedance, linearity, and gain stability are all reduced by  $A_{VOL}\beta$  with the use of negative feedback.

Another useful approximation is developed as follows. A rearrangement of Eq. 1-9 is:

$$\frac{A_{VOL}}{G_{CL}} = 1 + A_{VOL}\beta \quad \text{Eq. 1-13}$$

So, for high values of  $A_{VOL}\beta$ ,

$$\frac{A_{VOL}}{G_{CL}} \approx A_{VOL}\beta \quad \text{Eq. 1-14}$$

Consequently, in a given feedback circuit the loop gain,  $A_{VOL}\beta$ , is approximately the numeric ratio (or difference, in dB) of the amplifier open-loop gain to the circuit closed-loop gain.

This loop gain discussion emphasizes that, indeed, loop gain is a very significant factor in predicting the performance of closed-loop operational amplifier circuits. The open-loop gain required to obtain an adequate amount of loop gain will, of course, depend on the desired closed-loop gain.

For example, using Eq. 1-14, an amplifier with  $A_{VOL} = 20,000$  will have an  $A_{VOL}\beta \approx 2000$  for a closed-loop gain of 10, but the loop gain will be only 20 for a closed-loop gain of 1000. The first situation implies an amplifier-related gain error on the order of  $\approx 0.05\%$ , while the second would result in about 5% error. Obviously, the higher the required gain, the greater will be the required open-loop gain to support an  $A_{VOL}\beta$  for a given accuracy.

## Frequency Dependence of Loop Gain

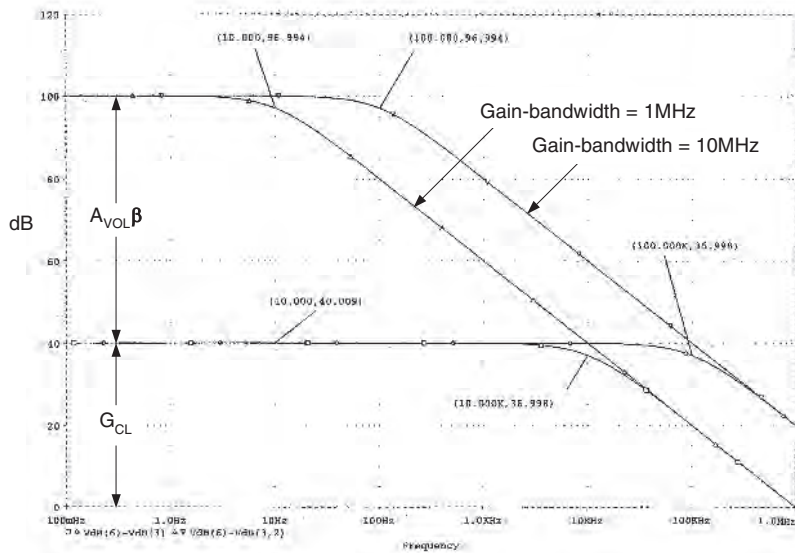
Thus far, it has been assumed that amplifier open-loop gain is independent of frequency. Unfortunately, this isn't the case. Leaving the discussion of the effect of open-loop response on bandwidth and dynamic errors until later, let us now investigate the general effect of frequency response on loop gain and static errors.

The open-loop frequency response for a typical operational amplifier with superimposed closed-loop amplifier response for a gain of 100 (40 dB), illustrates graphically these results in Figure 1-7. In these Bode plots, subtraction on a logarithmic scale is equivalent to normal division of numeric data.<sup>5</sup> Today, op amp open-loop gain and loop gain parameters are typically given in dB terms, thus this display method is convenient.

A few key points evolve from this graphic figure, which is a simulation involving two hypothetical op amps, both with a dc/low frequency gain of 100 dB (100 kV/V). The first has a gain-bandwidth of 1 MHz, while the gain-bandwidth of the second is 10 MHz.

- The open-loop gain  $A_{VOL}$  for the two op amps is noted by the two curves marked 1 MHz and 10 MHz, respectively. Note that each has a  $-3$  dB corner frequency associated with it, above which the open-loop gain falls at 6 dB/octave. These corner frequencies are marked at 10 Hz and 100 Hz, respectively, for the two op amps.
- At any frequency on the open-loop gain curve, the numeric product of gain  $A_{VOL}$  and frequency,  $f$ , is a constant (10,000 V/V at 100 Hz equates to 1 MHz). This, by definition, is characteristic of a constant gain-bandwidth product amplifier. All *voltage feedback* op amps behave in this manner.

<sup>5</sup> The log-log displays of amplifier gain (and phase) versus frequency are called *Bode* plots. This graphic technique for display of feedback amplifier characteristics, plus definitions for feedback amplifier stability were pioneered by Hendrick W. Bode of Bell Labs (see Reference 6).



**Figure 1-7: Op amp closed-loop gain and loop gain interactions with typical open-loop responses**

- $A_{VOL}\beta$  in dB is the difference between open-loop gain and closed-loop gain, as plotted on log-log scales. At the lower frequency point marked,  $A_{VOL}\beta$  is thus 60 dB.
- $A_{VOL}\beta$  decreases with increasing frequency, due to the decrease of  $A_{VOL}$  above the open-loop corner frequency. At 100 Hz for example, the 1 MHz gain-bandwidth amplifier shows an  $A_{VOL}\beta$  of only 80 dB – 40 dB = 40 dB.
- $A_{VOL}\beta$  also decreases for higher values of closed-loop gain. Other, higher closed-loop gain examples (not shown) would decrease  $A_{VOL}\beta$  to less than 60 dB at low frequencies.
- $G_{CL}$  depends primarily on the ratio of the feedback components,  $Z_F$  and  $Z_G$ , and is relatively independent of  $A_{VOL}$  (apart from the errors discussed above, which are inversely proportional to  $A_{VOL}\beta$ ). In this example  $1/\beta$  is 100, or 40 dB, and is so marked at 10 Hz. Note that  $G_{CL}$  is flat with increasing frequency, up until that frequency where  $G_{CL}$  intersects the open-loop gain curve, and  $A_{VOL}\beta$  drops to zero.
- At this point where the closed-loop and open-loop curves intersect, the loop gain is by definition zero, which implies that beyond this point there is no negative feedback. Consequently, closed-loop gain is equal to open-loop gain for further increases in frequency.
- Note that the 10 MHz gain-bandwidth op amp allows a 10× increase in closed-loop bandwidth, as can be noted from the –3 dB frequencies; that is 100 kHz versus 10 kHz for the 10 MHz versus the 1 MHz gain-bandwidth op amp.

Figure 1-7 illustrates that the high open-loop gain figures typically quoted for op amps can be somewhat misleading. As noted, beyond a few Hz, the open-loop gain falls at 6 dB/octave. Consequently, closed-loop gain stability, output impedance, linearity and other parameters dependent upon loop gain are degraded at higher frequencies. One of the reasons for having dc gain as high as 100 dB and bandwidth as wide as several MHz, is to obtain adequate loop gain at frequencies even as low as 100 Hz.



A direct approach to improving loop gain at high frequencies, other than by increasing open-loop gain, is to increase the amplifier open-loop bandwidth. Figure 1-7 shows this in terms of two simple examples. It should be borne in mind however that op amp gain-bandwidths available today extend to the hundreds of MHz, allowing video and high-speed communications circuits to fully exploit the virtues of feedback.

## Op Amp Common-Mode Dynamic Range(s)

As a point of departure from the idealized circuits above, some practical basic points are now considered. Among the most evident of these is the allowable input and output dynamic ranges afforded in a real op amp. This obviously varies with not only the specific device, but also the supply voltage. While we can always optimize this performance point with device selection, more fundamental considerations come first.

Any real op amp will have a finite voltage range of operation, at both input and output. In modern system designs, supply voltages are dropping rapidly, and 3 V – 5 V total supply voltages are now common. This is a far cry from supply systems of the past, which were typically  $\pm 15$  V (30 V total). Obviously, if designs are to accommodate a 3 V – 5 V supply, careful consideration must be given to maximizing dynamic range, by choosing a correct device. Choosing a device will be in terms of exact specifications, but first and foremost it should be in terms of the basic topologies used within it.

## Output Dynamic Range

Figure 1-8 is a general illustration of the limitations imposed by input and output dynamic ranges of an op amp, related to both supply rails. Any op amp will always be powered by two supply potentials, indicated by the positive rail,  $+V_S$ , and the negative rail,  $-V_S$ . We will define the op amp's input and output CM range in terms of how closely it can approach these two rail voltage limits.

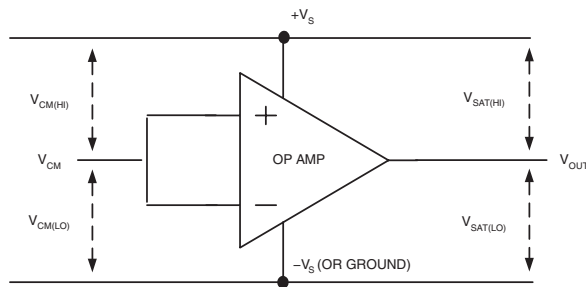


Figure 1-8: Op amp input and output common-mode ranges

At the output,  $V_{OUT}$  has two rail-imposed limits, one high or close to  $+V_S$ , and one low, or close to  $-V_S$ . Going high, it can range from an upper saturation limit of  $+V_S - V_{SAT(HI)}$  as a positive maximum. For example if  $+V_S$  is 5 V, and  $V_{SAT(HI)}$  is 100 mV, the upper  $V_{OUT}$  limit or positive maximum is 4.9 V. Similarly, going low it can range from a lower saturation limit of  $-V_S + V_{SAT(LO)}$ . So, if  $-V_S$  is ground (0 V) and  $V_{SAT(LO)}$  is 50 mV, the lower limit of  $V_{OUT}$  is simply 50 mV.

Obviously, the internal design of a given op amp will impact this output CM dynamic range, since, when so necessary, the device itself must be designed to minimize both  $V_{SAT(HI)}$  and  $V_{SAT(LO)}$ , to maximize the output dynamic range. Certain types of op amp structures are so designed, and these are generally associated with designs expressly for *single-supply* systems. This is covered in detail later within the chapter.

## Input Dynamic Range

At the input, the CM range useful for  $V_{IN}$  also has two rail-imposed limits, one high or close to  $+V_S$ , and one low, or close to  $-V_S$ . Going high, it can range from an upper CM limit of  $+V_S - V_{CM(HI)}$  as a positive maximum. For example, again using the  $+V_S = 5\text{ V}$  example case, if  $V_{CM(HI)}$  is 1 V, the upper  $V_{IN}$  limit or positive CM maximum is  $+V_S - V_{CM(HI)}$ , or 4 V.

Figure 1-9 illustrates by way of a hypothetical op amp's data how  $V_{CM(HI)}$  could be specified, as shown in the upper curve. This particular op amp would operate for  $V_{CM}$  inputs *lower* than the curve shown.

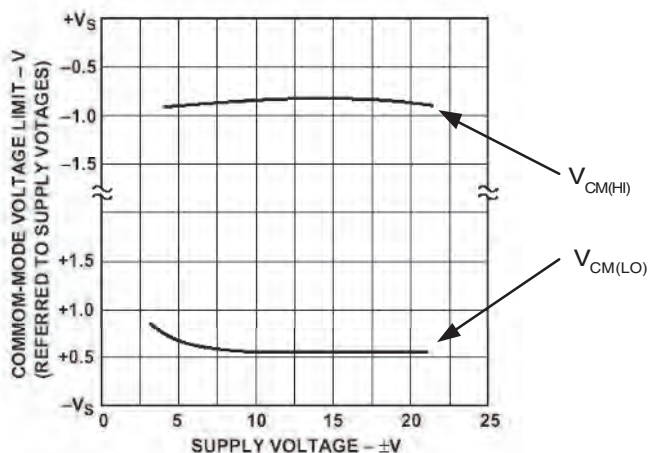


Figure 1-9: A graphical display of op amp input common mode range

In practice the input CM range of real op amps is typically specified as a *range of voltages*, not necessarily referenced to  $+V_S$  or  $-V_S$ . For example, a typical  $\pm 15\text{ V}$  operated dual supply op amp would be specified for an operating CM range of  $\pm 13\text{ V}$ . Going low, there will also be a lower CM limit. This can be generally expressed as  $-V_S + V_{CM(LO)}$ , which would appear in a graph such as Figure 1-9 as the lower curve, for  $V_{CM(LO)}$ . If this were again a  $\pm 15\text{ V}$  part, this could represent typical performance.

To use a single-supply example, for the  $-V_S = 0\text{ V}$  case, if  $V_{CM(LO)}$  is 100 mV, the lower CM limit will be  $0\text{ V} + 0.1\text{ V}$ , or simply 0.1 V. Although this example illustrates a lower CM range within 100 mV of  $-V_S$ , it is actually much more typical to see single-supply devices with lower or upper CM ranges, which *include* the supply rail.

In other words,  $V_{CM(LO)}$  or  $V_{CM(HI)}$  is 0 V. There are also single-supply devices with CM ranges that include *both* rails. More often than not, however, single-supply devices will not offer graphical data such as Figure 1-9 for CM limits, but will simply cover performance with a tabular range of specified voltage.

## Functionality Differences of Dual-Supply and Single-Supply Devices

There are two major classes of op amps, the choice of which determines how well the selected part will function in a given system. Traditionally, many op amps have been designed to operate on a dual power supply system, which has typically been  $\pm 15$  V. This custom has been prevalent since the earliest IC op amps days, dating back to the mid-sixties. Such devices can accommodate input/output ranges of  $\pm 10$  V (or slightly more), but when operated on supplies of appreciably lower voltage, for example  $\pm 5$  V or less, they suffer either loss of performance, or simply don't operate at all. This type of device is referenced here as a *dual-supply* op amp design. This moniker indicates that it performs optimally on dual voltage systems only, typically  $\pm 15$  V. It may or may not also work at appreciably lower voltages.

Figure 1-10 illustrates in a broad overview the relative functional performance differences that distinguish the dual-supply versus single-supply op amp classes. This table is arranged to illustrate various general performance parameters, with an emphasis on the contrast between single- and dual-supply devices. Which particular performance area is more critical will determine which type of device will be the better system choice.

PERFORMANCE PARAMETER	DUAL SUPPLY	SINGLE SUPPLY
SUPPLY LIMITATIONS	Best >10V, Limited <10V	Best <10V, Limited >10V
OUTPUT V RANGE	– Limited	+ Greatest
INPUT V RANGE	– Limited	+ Greatest
TOTAL DYNAMIC RANGE	+ Greatest	– Least
V & I OUTPUT PRECISION	+ Greater	– Less
LOAD IMMUNITY	+ Greatest	– Least
VARIETY AVAILABLE	+ Greater	– Less (growing)

**Figure 1-10: Comparison of relative functional performance differences between single and dual-supply op amps**

More recently, with increasing design attention to lower overall system power and the use of single rail power, the single-supply op amp has come into vogue. This has not been without good reason, as the virtues of using single supply rails can be quite compelling. A review of Figure 1-10 illustrates key points of the dual versus single supply op amp question.

In terms of *supply voltage limitations*, there is a crossover region in terms of overall utility, which occurs around 10 V of total supply voltage.

For example, single-supply devices tend to excel in terms of their *input and output voltage dynamic ranges*. Note that in Figure 1-10 a maximum range is stated as a percentage of available supply. Single-supply parts operate better in this regard, because they are internally designed to maximize these respective ranges. For example, it is not unusual for a device operating from 5 V to swing 4.8 V at the output, and so on.

But, rather interestingly, such devices are also usually restricted to lower supply ranges (only), so their upper dynamic range in absolute terms is actually more limited. For example, a traditional  $\pm 15$  V

dual-supply device can typically swing 20 V p-p, or more than four times that of a 5 V single-supply part. If the *total dynamic range* is considered (assuming an identical input noise), the dual-supply operated part will have four times (or 12 dB) greater dynamic range than that of the 5 V operated part. Or, stated in another way, the input errors of a real part such as noise, drift, and so forth, become four times more critical (relatively speaking), when the output dynamic range is reduced by a factor of 4. Note that these comparisons do not involve any actual device specifications, *they are simply system-based observations*. Device specifications are covered later in this chapter.

In terms of total *voltage and current output*, dual-supply parts tend to offer more in absolute terms, since single-supply parts are usually designed not just for low operating voltage ranges, but also for more modest current outputs.

In terms of *precision*, the dual-supply op amp has long been favored by designers for highest overall precision. However, this status quo is now beginning to be challenged, by such single-supply parts as the truly excellent chopper-stabilized op amps. With more and more new op amps being designed for single-supply use, high precision is likely to become an ever-increasing strength of this category.

*Load immunity* is often an application problem with single-supply parts, as many of them use common-emitter or common-source output stages, to maximize signal swing. Such stages are typically much more load sensitive than the classic common-collector stages generally used in dual-supply op amps.

There is now a greater *variety* of dual-supply op amps available. However, this is at least in part due to the ~30-year head start they have been enjoying. Currently, new op amp designs are increasingly oriented around one or more aspects of single-supply compatibility, with strong trends toward lower supply voltages, smaller packages, and so forth.

## Device Selection Drivers

As the op amp design process is begun, it is useful to keep in mind the fact that there are several selection *drivers*, which can dictate priorities. This is illustrated by Figure 1-11.

FUNCTION	PERFORM	PACKAGE	MARKET
Single, Dual, Quad	Precision	Type	Cost
Single Or Dual Supply	Speed	Size	Availability
Supply Voltage	Distortion, Noise	Footprint	
	Low Bias Current		
	Power		

Figure 1-11: Some op amp selection drivers

Actually, any *single* heading along the top of this chart can, in fact, be the dominant selection driver and take precedence over all of the others. In the early days of op amp design, when such things as supply range, package type, and so forth, were fairly narrow in spread, performance was usually the major driver. Of course, it is still very much so and will always be. But, today's systems are much more compact and lower in power, so things like package type, size, supply range, and multiple devices can often be major drivers of selection. As one example, if the only available supply voltage is 3 V, look at 3 V compatible devices first, and then fill other performance parameters as you can.

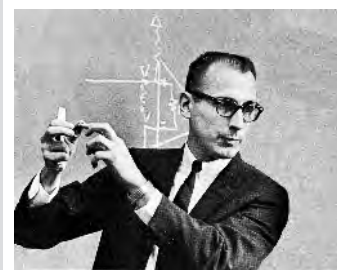
As another example, one coming from another perspective, sometimes all-out performance can drive everything else. An ultralow, non-negotiable input current requirement can drive not only the type of amplifier, but also its package (a FET input device in a glass-sealed hermetic package may be optimum). Then, everything else follows from there. Similarly, high power output may demand a package capable of several watts dissipation; in which case, find the power handling device and package first, and then proceed accordingly.

At this point, the concept of these “selection drivers” is still quite general. The following sections of the chapter introduce device types, which supplement this with further details of a realistic selection process.

### Classic Cameo

#### **Ray Stata Publications Establish ADI Applications Work**

In January of 1965 Analog Devices Inc. (ADI) was founded by Matt Lorber and Ray Stata. Operating initially from Cambridge, MA, modular op amps were the young ADI’s primary product. In those days, Ray Stata did more than administrative tasks. He served in sales and marketing roles, and wrote many op amp applications articles. Even today, some of these are still available to ADI customers.



One very early article set was a two part series done for **Electromechanical Design**, which focused on clear, down-to-earth explanation of op amp principles.<sup>1</sup>

A second article for the new ADI publication **Analog Dialogue** was titled “Operational Integrators,” and outlined various errors that plague integrators (including capacitor errors).<sup>2</sup>

A third impact article was also done for **Analog Dialogue**, titled “User’s Guide to Applying and Measuring Operational Amplifier Specifications.”<sup>3</sup> As the title denotes, this was a comprehensive guide to aid the understanding of op amp specifications, and also showed how to test them.

Ray authored an Applications Manual for the 201, 202, 203 and 210 series of chopper op amps.<sup>4</sup>

Ray was also part of the **EEE** “Speaks Out” series of article-interviews, where he outlined some of the subtle ways that op amp specs and behavior can trap unwary users (above photo from that article).<sup>5</sup>

Although ADI today makes many other products, those early op amps were the company’s roots.

<sup>1</sup> Ray Stata, “Operational Amplifiers – Parts I and II,” **Electromechanical Design**, Sept., Nov., 1965.

<sup>2</sup> Ray Stata, “Operational Integrators,” **Analog Dialogue**, Vol. 1, No. 1, April, 1967. See also ADI AN357.

<sup>3</sup> Ray Stata, “User’s Guide to Applying and Measuring Operational Amplifier Specifications,” **Analog Dialogue**, Vol. 1, No. 3, September 1967. See also ADI AN356.

<sup>4</sup> Ray Stata, **Applications Manual for 201, 202, 203 and 210 Chopper Op Amps**, ADI, 1967.

<sup>5</sup> “Ray Stata Speaks Out on ‘What’s Wrong with Op Amp Specs’,” **EEE**, July 1968.

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1. John R. Ragazzini, Robert H. Randall and Frederick A. Russell, "Analysis of Problems in Dynamics by Electronic Circuits," **Proceedings of the IRE**, Vol. 35, May 1947, pp. 444–452.
2. Walter Borlase, **An Introduction to Operational Amplifiers (Parts 1–3)**, September 1971, Analog Devices Seminar Notes, Analog Devices, Inc.
3. Karl D. Swartzel, Jr. "Summing Amplifier," **US Patent 2,401,779**, filed May 1, 1941, issued June 11, 1946.
4. Frederick E. Terman, "Feedback Amplifier Design," **Electronics**, Vol. 10, No. 1, January 1937, pp. 12–15, 50.
5. Julian M. West, "Wave Amplifying System," **US Patent 2,196,844**, filed April 26, 1939, issued April 9, 1940.
6. Hendrick W. Bode, "Relations Between Attenuation and Phase In Feedback Amplifier Design," **Bell System Technical Journal**, Vol. 19, No. 3, July, 1940. See also: "Amplifier," **US Patent 2,173,178**, filed June 22, 1937, issued July 12, 1938.
7. Ray Stata, "Operational Amplifiers-Parts I and II," **Electromechanical Design**, September, November 1965.
8. Dan Sheingold, Ed., **Applications Manual for Operational Amplifiers for Modeling, Measuring, Manipulating, and Much Else**, George A. Philbrick Researches, Inc., Boston, MA, 1965. See also **Applications Manual for Operational Amplifiers for Modeling, Measuring, Manipulating, and Much Else, 2<sup>nd</sup> Ed.**, Philbrick/Nexus Research, Dedham, MA, 1966, 1984.
9. Walter G. Jung, **IC Op Amp Cookbook, 3<sup>rd</sup> Ed.**, Prentice-Hall PTR, 1986, 1997, ISBN: 0-13-889601-1.
10. Walt Kester, Editor, **Linear Design Seminar**, Analog Devices, Inc., 1995, ISBN: 0-916550-15-X.
11. Sergio Franco, **Design With Operational Amplifiers and Analog Integrated Circuits, 2<sup>nd</sup> Ed.** (Sections 1.2 – 1.4), McGraw-Hill, 1998, ISBN: 0-07-021857-9.

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# Op Amp Topologies

Walt Kester, Walt Jung, James Bryant

The previous section examined op amps without regard to their internal circuitry. In this section the two basic op amp topologies—voltage feedback (VFB) and current feedback (CFB)—are discussed in more detail, leading up to a detailed discussion of the actual circuit structures in Section 1-3.

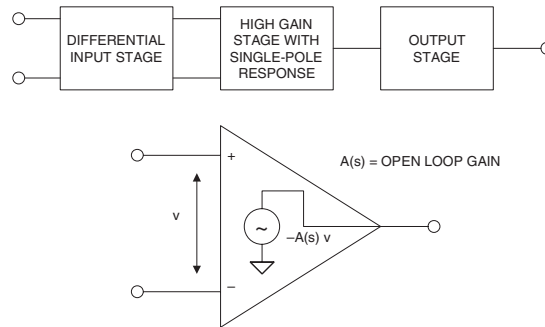


Figure 1-12: Voltage feedback (VFB) op amp

Although not explicitly stated, the previous section focused on the voltage feedback op amp and the related equations. In order to reiterate, the basic voltage feedback op amp is repeated here in Figure 1-12 (without the feedback network) and in Figure 1-13 (with the feedback network).

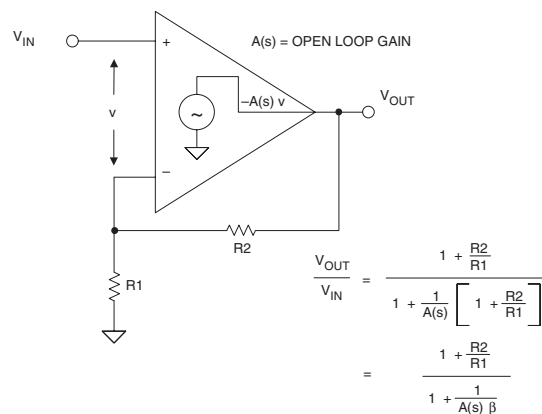


Figure 1-13: Voltage feedback op amp with feedback network connected

It is important to note that the error signal developed because of the feedback network and the finite open-loop gain  $A(s)$  is in fact a small voltage,  $v$ .



## Current Feedback Amplifier Basics

The basic *current feedback* amplifier topology is shown in Figure 1-14. Notice that within the model, a unity gain buffer connects the noninverting input to the inverting input. In the ideal case, the output impedance of this buffer is zero ( $R_O = 0$ ), and the error signal is a small current,  $i$ , which flows into the inverting input. The error current,  $i$ , is mirrored into a high impedance,  $T(s)$ , and the voltage developed across  $T(s)$  is equal to  $T(s) \cdot i$ . (The quantity  $T(s)$  is generally referred to as the *open-loop transimpedance gain*.)

This voltage is then buffered and connected to the op amp output. If  $R_O$  is assumed to be zero, it is easy to derive the expression for the closed-loop gain,  $V_{OUT}/V_{IN}$ , in terms of the  $R_1$ - $R_2$  feedback network and the *open-loop* transimpedance gain,  $T(s)$ . The equation can also be derived quite easily for a finite  $R_O$ , and Figure 1-14 gives both expressions.

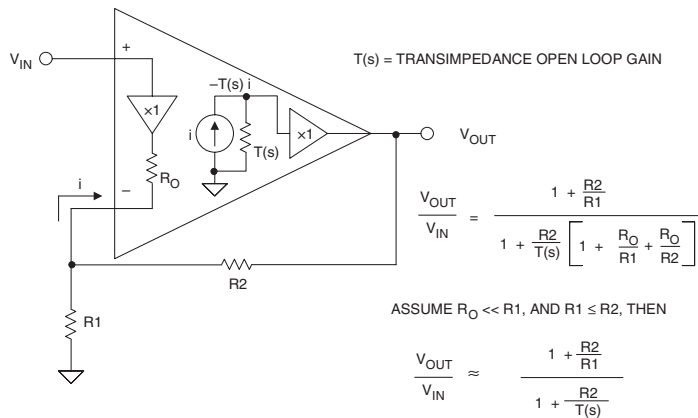


Figure 1-14: Current feedback (CFB) op amp topology

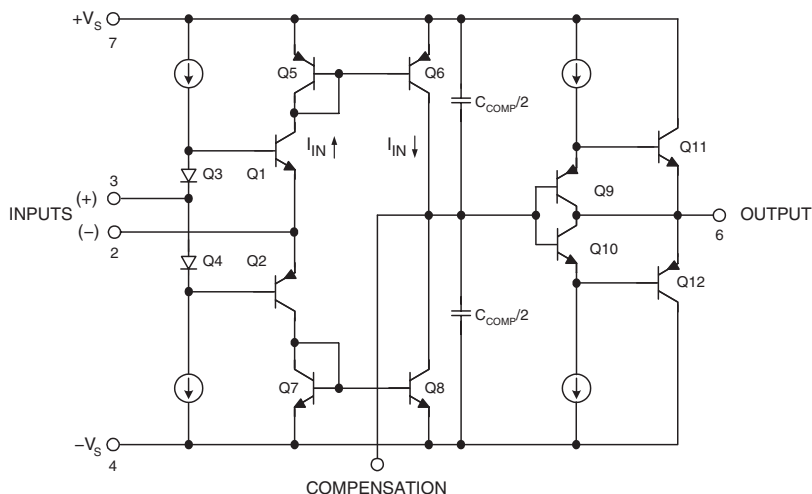
At this point it should be noted that current feedback op amps are often called *transimpedance* op amps, because the *open-loop* transfer function is in fact an impedance as described above. However, the term *transimpedance amplifier* is often applied to more general circuits such as current-to-voltage (I/V) converters, where either CFB or VFB op amps can be used. Therefore, some caution is warranted when the term *transimpedance* is encountered in a given application. On the other hand, the term *current feedback op amp* is rarely confused and is the preferred nomenclature when referring to op amp topology.

From this simple model, several important CFB op amp characteristics can be deduced.

- Unlike VFB op amps, CFB op amps *do not have balanced inputs*. Instead, the noninverting input is high impedance, and the inverting input is low impedance.
- The open-loop gain of CFB op amps is measured in units of  $\Omega$  (transimpedance gain) rather than V/V as for VFB op amps.
- For a fixed value feedback resistor  $R_2$ , the closed-loop gain of a CFB can be varied by changing  $R_1$ , without significantly affecting the closed-loop bandwidth. This can be seen by examining the simplified equation in Figure 1-14. The denominator determines the overall frequency response; and if  $R_2$  is constant, then  $R_1$  of the numerator can be changed (thereby changing the gain) without affecting the denominator—hence the bandwidth remains relatively constant.

The CFB topology is primarily used where the ultimate in high speed and low distortion is required. The fundamental concept is based on the fact that in bipolar transistor circuits currents can be switched faster than voltages, all other things being equal. A more detailed discussion of CFB op amp ac characteristics can be found in Section 1-5.

Figure 1-15 shows a simplified schematic of an early IC CFB op amp, the AD846—introduced by Analog Devices in 1988 (see Reference 1). Notice that full advantage is taken of the complementary bipolar (CB) process which provides well matched high  $f_t$  PNP and NPN transistors.



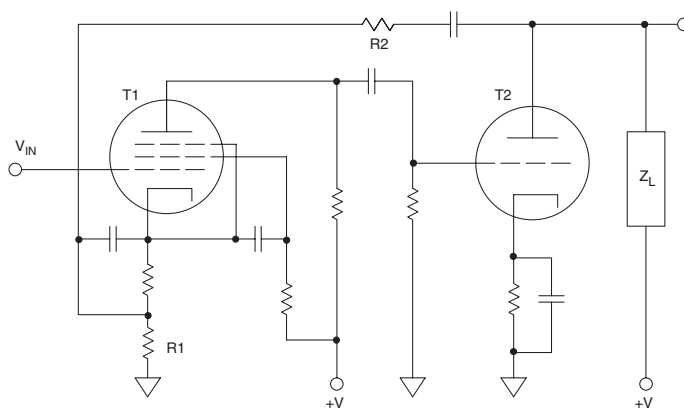
**Figure 1-15: AD846 current feedback op amp (1988)**

Transistors Q1–Q2 buffer the noninverting input (Pin 3) and drive the inverting input (Pin 2). Q5–Q6 and Q7–Q8 act as current mirrors that drive the high impedance node. The  $C_{\text{COMP}}$  capacitor provides the dominant pole compensation; and Q9, Q10, Q11, and Q12 comprise the output buffer. In order to take full advantage of the CFB architecture, a high speed complementary bipolar (CB) IC process is required. With modern IC processes, this is readily achievable, allowing direct coupling in the signal path of the amplifier.

However, the basic concept of current feedback can be traced all the way back to early vacuum tube feedback circuitry, which used negative feedback to the input tube cathode. This use of the cathode for feedback would be analogous to the CFB op amp's low impedance (–) input, in Figure 1-15.

## Current Feedback Using Vacuum Tubes

Figure 1-16 is an adaptation from a 1937 article on feedback amplifiers by Frederick E. Terman (see Reference 2). Notice that the ac-coupled R2 feedback resistor for this two-stage amplifier is connected to the low impedance cathode of T1, the pentode vacuum tube input stage. Similar examples of early tube circuits using cathode feedback can be found in Reference 3.



Adapted from: Frederick E. Terman, "Feedback Amplifier Design,"  
Electronics, January 1937, pp. 12-15, 50.

**Figure 1-16: A 1937 vacuum tube feedback circuit designed by Frederick E. Terman, using current feedback to the low impedance input cathode (adapted from Reference 2)**

Dc-coupled op amp design using vacuum tubes was difficult for numerous reasons. One reason was a lack of suitable level shifters. Multistage op amps either required extremely high supply voltages or suffered gain loss because of resistive level shifters. In a 1941 article, Stewart E. Miller describes how to use gas discharge tubes as level shifters in several vacuum tube amplifier circuits (see Reference 4). A circuit of particular interest is shown in Figure 1-17.

In the Figure 1-17 reproduction of Miller's circuit, the R2 feedback resistor and the R1 gain setting resistor are labeled for clarity, and it can be seen that feedback is to the low impedance cathode of the input tube. The author suggests that the closed-loop gain of the amplifier can be adjusted from 72 dB–102 dB, by varying the R1 gain-setting resistor from 37.4  $\Omega$  to 1.04  $\Omega$ .

What is really interesting about the Miller circuit is its frequency response, which is reproduced in Figure 1-18. Notice that the closed-loop bandwidth is nearly independent of the gain setting, and the circuit certainly does not exhibit a constant gain-bandwidth product as would be expected for a traditional VFB op amp.

For a gain of 72 dB, the bandwidth is about 30 kHz, and for a gain of 102 dB (30 dB increase), the bandwidth only drops to ~15 kHz. With a 72 dB gain at 30 kHz VFB op amp, bandwidth would be expected to drop 5 octaves to ~0.9 kHz for 102 dB of gain.

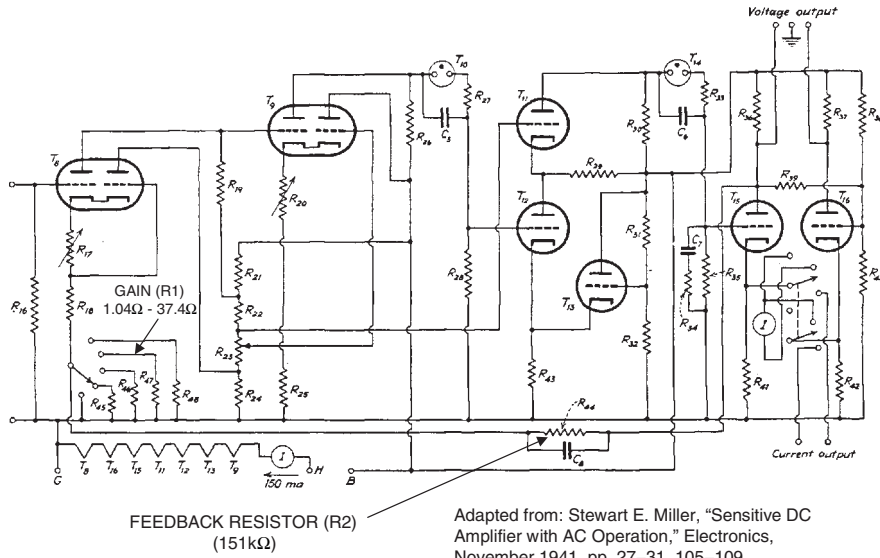
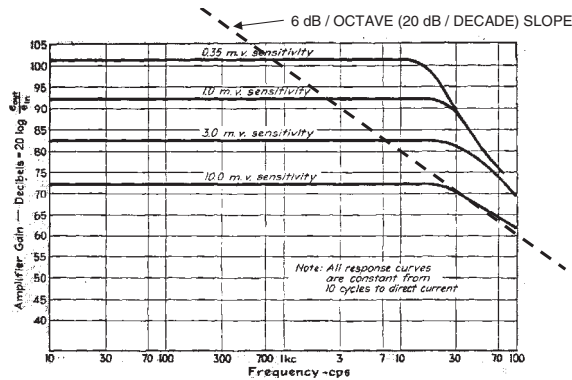


Figure 1-17: A 1941 vacuum tube feedback circuit using current feedback

To clarify this point on bandwidth, a standard VFB op amp 6 dB/octave (20 dB/decade) slope has been added to Figure 1-18 for reference.

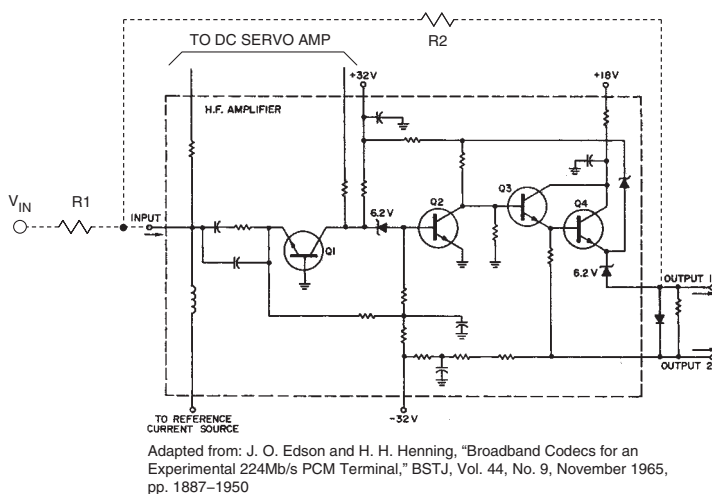
Although there is no mention of the significance of this within the text of the actual article, it nevertheless illustrates a popular application of CFB behavior, in the design of high speed programmable gain amplifiers with relatively constant bandwidth.



Adapted from: Stewart E. Miller, "Sensitive DC Amplifier with AC Operation," Electronics, November 1941, pp. 27-31, 105-109

Figure 1-18: A 1941 feedback circuit shows characteristic CFB gain-bandwidth relationship

When transistor circuits ultimately replaced vacuum tube circuits between the late 1950s and the mid-1960s, the current feedback architecture became popular for certain high speed op amps. Figure 1-19 shows a fast-settling op amp designed at Bell Labs in 1965, for use as a building block in high speed A/D converters (see Reference 5).



**Figure 1-19: A 1965 solid- state current feedback op amp design from Bell Labs**

The circuit shown is a composite amplifier containing a high speed ac amplifier (shown inside the dotted outline) and a separate dc servo amplifier loop (not shown). The feedback resistor R2 is ac coupled to the low impedance emitter of transistor Q1. The circuit design was somewhat awkward because of the lack of good high frequency PNP transistors, and it also required zener diode level shifters, and nonstandard supplies.

Hybrid circuit manufacturing technology, which was well established by the 1980s, allowed the use of fast, relatively well-matched NPN and PNP transistors, to realize CFB op amps. The Analog Devices' AD9610 and AD9611 hybrids were good examples of these devices introduced in the mid-1980s.

With the development of high speed complementary bipolar IC processes in the 1980s (see Reference 6) it became possible to realize completely dc-coupled current feedback op amps using PNP and NPN transistors such as the Analog Devices' AD846, introduced in 1988 (Figure 1-15). Device matching and clever circuit design techniques give these modern IC CFB op amps excellent ac and dc performance without a requirement for separate level shifters, awkward supply voltages, or separate dc servo loops.

Various patents have been issued for these types of designs (see References 7 and 8, for example), but it should be remembered that the fundamental concepts were established decades earlier.

## References: Op Amp Topologies

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# *Op Amp Structures*

*Walt Kester, Walt Jung, James Bryant*

This section describes op amps in terms of their *structures*, and Section 1-4 discusses op amp *specifications*. It is hard to decide which to discuss first, since discussion of specifications, to be useful, entails reference to structures, and discussion of structures likewise requires reference to the performance feature that they are intended to optimize.

Since the majority of readers will have at least some familiarity with operational amplifiers and their specifications, we shall discuss structures first, and assume that readers will have at least a first-order idea of the definitions of the various specifications. Where this assumption proves ill-founded, the reader should look ahead to the next section to verify any definitions required.

Because single-supply devices permeate practically all modern system designs, the related design issues are integrated into the following op amp structural discussions.

## *Single-Supply Op Amp Issues*

Over the last several years, single-supply operation has become an increasingly important requirement because of market demands. Automotive, set-top box, camera/camcorder, PC, and laptop computer applications are demanding IC vendors to supply an array of linear devices that operate on a single-supply rail, with the same performance of dual supply parts. Power consumption is now a key parameter for line or battery-operated systems, and in some instances, more important than cost. This makes low voltage/low supply current operation critical; at the same time, however, accuracy and precision requirements have forced IC manufacturers to meet the challenge of “doing more with less” in their amplifier designs.

In a single-supply application, the most immediate effect on the performance of an amplifier is the reduced input and output signal range. As a result of these lower input and output signal excursions, amplifier circuits become more sensitive to internal and external error sources. Precision amplifier offset voltages on the order of 0.1 mV are less than a 0.04 LSB error source in a 12-bit, 10 V full-scale system. In a single-supply system, however, a “rail-to-rail” precision amplifier with an offset voltage of 1 mV represents a 0.8 LSB error in a 5 V full-scale system (or 1.6 LSB for 2.5 V full-scale).

To keep battery current drain low, larger resistors are usually used around the op amp. Since the bias current flows through these larger resistors, they can generate offset errors equal to or greater than the amplifier’s own offset voltage.

Gain accuracy in some low voltage single-supply devices is also reduced, so device selection needs careful consideration. Many amplifiers with ~120 dB open-loop gains typically operate on dual supplies—for example OP07 types. However, many single-supply/rail-to-rail amplifiers for precision applications typically have open-loop gains between 25,000 and 30,000 under light loading ( $>10\text{ k}\Omega$ ). Selected devices, like the OP113/OP213/OP413 family, do have high open-loop gains ( $>120\text{ dB}$ ), for use in demanding applications. Another example would be the AD855x chopper-stabilized op amp series.

Many trade-offs are possible in the design of a single-supply amplifier circuit—speed versus power, noise versus power, precision versus speed and power, and so forth. Even if the noise floor remains constant (highly unlikely), the signal-to-noise ratio will drop as the signal amplitude decreases.



Besides these limitations, many other design considerations that are otherwise minor issues in dual-supply amplifiers now become important. For example, signal-to-noise (SNR) performance degrades as a result of reduced signal swing. “Ground reference” is no longer a simple choice, as one reference voltage may work for some devices, but not others. Amplifier voltage noise increases as operating supply current drops, and bandwidth decreases. Achieving adequate bandwidth and required precision with a somewhat limited selection of amplifiers presents significant system design challenges in single-supply, low power applications.

Most circuit designers take “ground” reference for granted. Many analog circuits scale their input and output ranges about a ground reference. In dual-supply applications, a reference that splits the supplies (0 V) is very convenient, as there is equal supply headroom in each direction, and 0 V is generally the voltage on the low impedance ground plane.

In single-supply/rail-to-rail circuits, however, the ground reference can be chosen anywhere within the supply range of the circuit, since there is no standard to follow. The choice of ground reference depends on the type of signals processed and the amplifier characteristics. For example, choosing the negative rail as the ground reference may optimize the dynamic range of an op amp whose output is designed to swing to 0 V. On the other hand, the signal may require level shifting in order to be compatible with the input of other devices (such as ADCs) that are not designed to operate at 0 V input.

Very early single-supply “zero-in, zero-out” amplifiers were designed on bipolar processes, which optimized the performance of the NPN transistors. The PNP transistors were either lateral or substrate PNPs with much less bandwidth than the NPNs. Fully complementary processes are now required for the new breed of single-supply/rail-to-rail operational amplifiers. These new amplifier designs don’t use lateral or substrate PNP transistors within the signal path, but incorporate parallel NPN and PNP input stages to accommodate input signal swings from ground to the positive supply rail. Furthermore, rail-to-rail output stages are designed with bipolar NPN and PNP common-emitter, or N-channel/P-channel common-source amplifiers whose collector-emitter saturation voltage or drain-source channel on resistance determine output signal swing as a function of the load current.

The characteristics of a single-supply amplifier input stage (common-mode rejection, input offset voltage and its temperature coefficient, and noise) are critical in precision, low voltage applications. Rail-rail input operational amplifiers must resolve small signals, whether their inputs are at ground, or in some cases near the amplifier’s positive supply. Amplifiers having a minimum of 60 dB common-mode rejection over the entire input common-mode voltage range from 0 V to the positive supply are good candidates. It is not necessary that amplifiers maintain common-mode rejection for signals beyond the supply voltages. *But, what is required is that they do not self-destruct for momentary overvoltage conditions.* Furthermore, amplifiers that have offset voltages less than 1 mV and offset voltage drifts less than 2  $\mu\text{V}/^\circ\text{C}$  are also very good candidates for precision applications. Since *input* signal dynamic range and SNR are equally if not more important than *output* dynamic range and SNR, precision single-supply/rail-to-rail operational amplifiers should have noise levels referred-to-input (RTI) less than 5  $\mu\text{V}$  p-p in the 0.1 Hz to 10 Hz band.

The need for rail-to-rail amplifier output stages is also driven by the need to maintain wide dynamic range in low supply voltage applications. A single-supply/rail-to-rail amplifier should have output voltage swings that are within at least 100 mV of either supply rail (under a nominal load). The output voltage swing is very dependent on output stage topology and load current.

Generally, the voltage swing of a good rail-to-rail output stage should maintain its rated swing for loads down to 10 k $\Omega$ . The smaller the  $V_{\text{OL}}$  and the larger the  $V_{\text{OH}}$ , the better. System parameters, such as “zero-scale” or “full-scale” output voltage, should be determined by an amplifier’s  $V_{\text{OL}}$  (for zero-scale) and  $V_{\text{OH}}$  (for full-scale).

- Single Supply Offers:
  - Lower Power
  - Battery-Operated Portable Equipment
  - Requires Only One Voltage
- Design Trade-Offs:
  - Reduced Signal Swing Increases Sensitivity to Errors Caused by Offset Voltage, Bias Current, Finite Open-Loop Gain, Noise, etc.
  - Must Usually Share Noisy Digital Supply
  - Rail-to-Rail Input and Output Needed to Increase Signal Swing
  - Precision Less than the best Dual Supply Op Amps but not Required for All Applications
  - Many Op Amps Specified for Single Supply, but do not have Rail-to-Rail Inputs or Outputs

**Figure 1-20: Single-supply op amp design issues**

Since the majority of single-supply data acquisition systems require at least 12-to 14-bit performance, amplifiers which exhibit an open-loop gain greater than 30,000 for all loading conditions are good choices in precision applications. Single-supply op amp design issues are summarized in Figure 1-20.

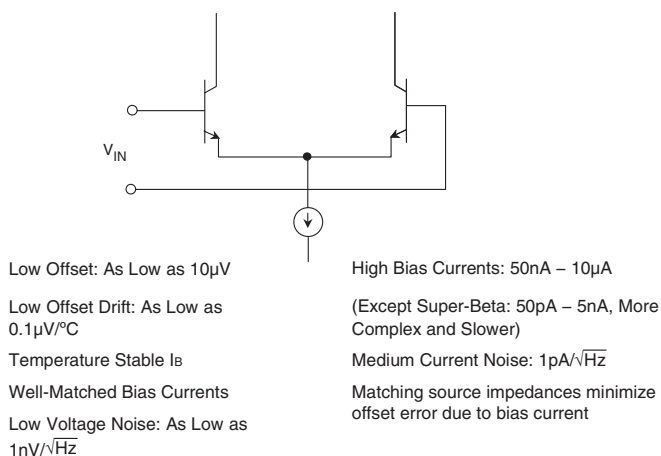
## Op Amp Input Stages

It is extremely important to understand input and output structures of op amps in order to properly design the required interfaces. For ease of discussion, the two can be examined separately, as there is no particular reason to relate them at this point.

### Bipolar Input Stages

The very common and basic bipolar input stage of Figure 1-21 consists of a “long-tailed pair” built with bipolar transistors. It has a number of advantages: it is simple, has very low offset, the bias currents in the inverting and noninverting inputs are well-matched and do not vary greatly with temperature. In addition, minimizing the initial offset voltage of a bipolar op amp by laser trimming also minimizes its drift over temperature. This architecture was used in the very earliest monolithic op amps such as the  $\mu\text{A}709$ . It is also used with modern high speed types, like the AD829 and AD8021.

Although NPN bipolars are shown, the concept also applies with the use of PNP bipolars.



**Figure 1-21: A bipolar transistor input stage**

The AD829, introduced in 1990, is shown in Figure 1-22. This op amp uses a bipolar differential input stage, Q1–Q2, which drives a “folded cascode” gain stage which consists of a fast pair of PNP transistors, Q3–Q4 (see Reference 1). These PNPs drive a current mirror that provides the differential-to-single-ended conversion. The output stage is a two-stage complementary emitter follower.

The AD829 is a wideband video amplifier with a 750 MHz uncompensated gain-bandwidth product, and it operates on  $\pm 5\text{ V}$  to  $\pm 15\text{ V}$  supplies. For added flexibility, the AD829 provides access to the internal compensation node ( $C_{\text{COMP}}$ ). This allows the user to customize frequency response characteristics for a particular application where the closed-loop gain is less than 20. The RC network connected between the output and the high impedance node helps maintain stability, when driving capacitive loads.

Input bias current is  $7\mu\text{A}$  maximum at  $25^\circ\text{C}$ , input voltage noise is  $1.7\text{ nV}/\sqrt{\text{Hz}}$ , and input current noise is  $1.5\text{ pA}/\sqrt{\text{Hz}}$ . Laser wafer trimming reduces the input offset voltage to  $0.5\text{ mV}$  maximum for the “A” grade. Typical input offset voltage drift is  $0.3\mu\text{V}/^\circ\text{C}$ .

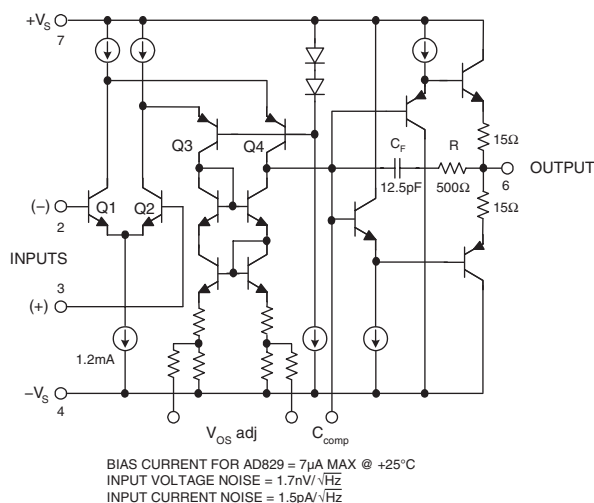


Figure 1-22: AD829 op amp simplified schematic

In an op amp input circuit such as Figure 1-22, the input bias current is the base current of the transistors comprising the long-tailed pair, Q1–Q2. It can be quite high, especially in high speed amplifiers, because the collector currents are high. It is typically  $\sim 3 \mu\text{A}$ , for the AD829. In amplifiers where the bias current is *uncompensated* (as true in this case), the bias current will be equal to one-half of the Q1–Q2 emitter current, divided by the  $H_{FE}$ .

The bias current of a simple bipolar input stage can be reduced by a couple of measures. One is by means of *bias current compensation*, to be described further below.

Another method of reducing bias current is by the use of *superbeta* transistors for Q1–Q2. Superbeta transistors are specially processed devices with a very narrow base region. They typically have a current gain of thousands or tens of thousands (rather than the more usual hundreds). Op amps with superbeta input stages have much lower bias currents, but they also have more limited frequency response.

Since the breakdown voltages of superbeta devices are quite low, they also require additional circuitry to protect the input stage from damage caused by overvoltage (for example, they wouldn't operate in the circuit of Figure 1-22).

Some examples of superbeta input bipolar op amps are the AD704/AD705/AD706 series, and the OP97/OP297/OP497 series (single, dual, quad). These devices have typical 25°C bias currents of 100 pA or less.

### Bias Current Compensated Bipolar Input Stage

A simple bipolar input stage such as used in Figure 1-22 exhibits high bias current because the currents seen externally are in fact the base currents of the two input transistors.

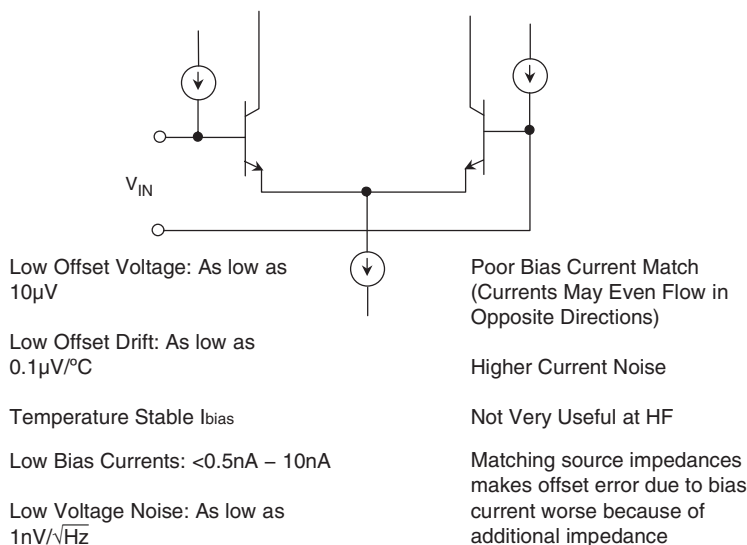


Figure 1-23: A bias current compensated bipolar input stage

By providing necessary bias currents via an internal current source, as in Figure 1-23, the only *external* current then flowing in the input terminals is the difference current between the base current and the current source, which can be quite small.

Most modern precision op amps use some means of internal bias current compensation; examples would be the familiar OP07 and OP27 series.

The well-known OP27 op amp family is good example of bias-compensated op amps (see References 2 and 3). The simplified schematic of the OP27, shown in Figure 1-24, shows that the multiple-collector transistor Q6 provides the bias current compensation for the input transistors Q1 and Q2. The “G” grade of the OP27

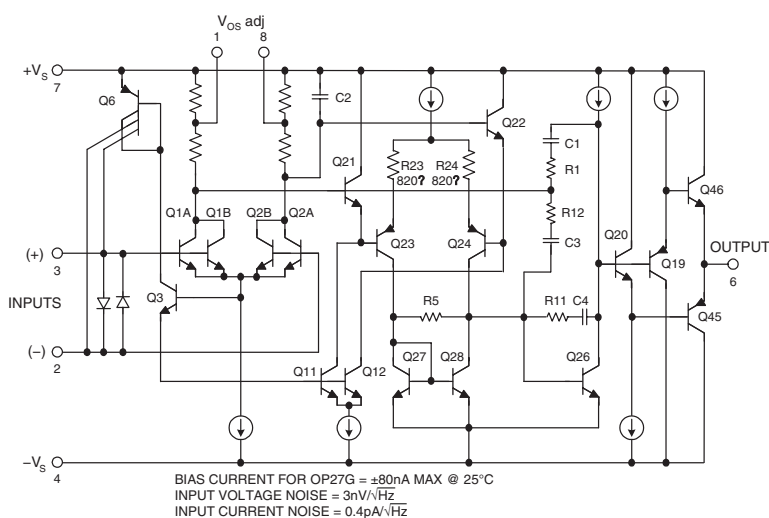


Figure 1-24: OP27 op amp uses bias current compensated input stage

has a maximum input bias current specification of  $\pm 80$  nA at 25°C. Input voltage noise is  $3 \text{ nV}/\sqrt{\text{Hz}}$ , and input current noise  $0.4 \text{ pA}/\sqrt{\text{Hz}}$ . Offset voltage trimming by “Zener-zapping” reduces the input offset voltage of the OP27 to 50  $\mu\text{V}$  maximum at 25°C for the “E” grade device (see Reference 4 for details of this trim method).

Bias-current-compensated input stages have many of the good features of the simple bipolar input stage, namely: low voltage noise, low offset, and low drift. Additionally, they have low bias current which is fairly stable with temperature. However, their current noise is not very good, and their bias current matching is poor.

These latter two undesirable side effects result from the external bias current being the *difference* between the compensating current source and the input transistor base current. Both of these currents inevitably have noise. Since they are uncorrelated, the two noises add in a root-sum-of-squares fashion (even though the dc currents subtract).

Since the resulting external bias current is the difference between two nearly equal currents, there is no reason why the net current should have a defined polarity. As a result, the bias currents of a bias-compensated op amp may not only be mismatched, they can actually flow in opposite directions. In most applications this isn’t important, but in some it can have unexpected effects. (For example, the droop of a sample-and-hold [SHA] built with a bias-compensated op amp may have either polarity.)

In many cases, the bias current compensation feature is not mentioned on an op amp data sheet, and a simplified schematic isn’t supplied. It is easy to determine if bias current compensation is used by examining the bias current specification. If the bias current is specified as a “ $\pm$ ” value, the op amp is most likely compensated for bias current.

Note that this can easily be verified by examining the *offset current* specification (the difference in the bias currents). If internal bias current compensation exists, the offset current will be of the same magnitude as the bias current. Without bias current compensation, the offset current will generally be at least a factor of 10 smaller than the bias current. Note that these relationships generally hold, regardless of the exact magnitude of the bias currents.

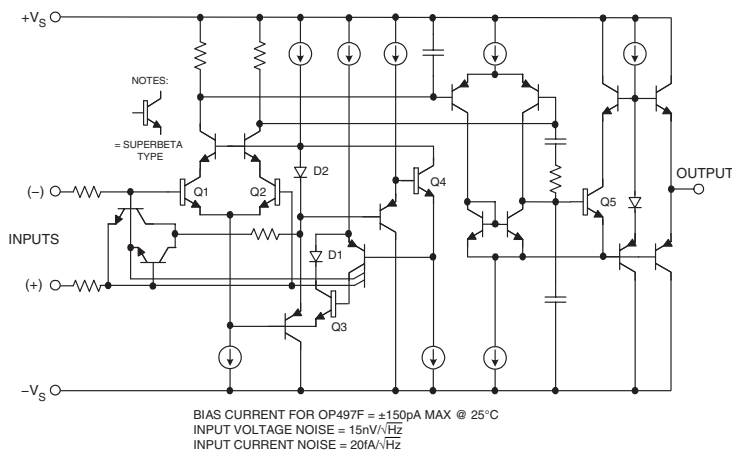
It is also a well-known fact that, within an op amp application circuit, the effects of bias current on the output offset voltage of an op amp can often be cancelled by making the source resistances at the two inputs equal. However, there is an important caveat here. The validity of this practice holds true only for bipolar input op amps *without* bias current compensation; that is, where the input currents are well matched. In a case of an op amp using internal bias current compensation, adding an extra resistance to either input will usually make the output offset worse.

### **Bias Current Compensated Superbeta Bipolar Input Stage**

As mentioned above, the OP97/297/OP497-series are high performance superbeta op amps, that also use input bias current compensation. As a result, their input bias currents are  $\pm 150$  pA max at 25°C. Note that in this case the “ $\pm$ ” prefix to the bias current magnitude indicates that the amplifier uses internal bias current compensation.

A simplified schematic of an OP97 (or one-quarter of the OP497) is shown in Figure 1-25. Note that the Q1–Q2 superbeta pair is protected against large destructive differential input voltages, by the use of both back-to-back diodes, and series current-limiting resistors. Note also that the Q1–Q2 superbeta pair is also protected against excessive collector voltage, by an elaborate bias and bootstrapping network.

As a result of these clamping and protection circuits, the input common-mode voltage of this op amp series can safely vary over the full range of the supply voltages used.



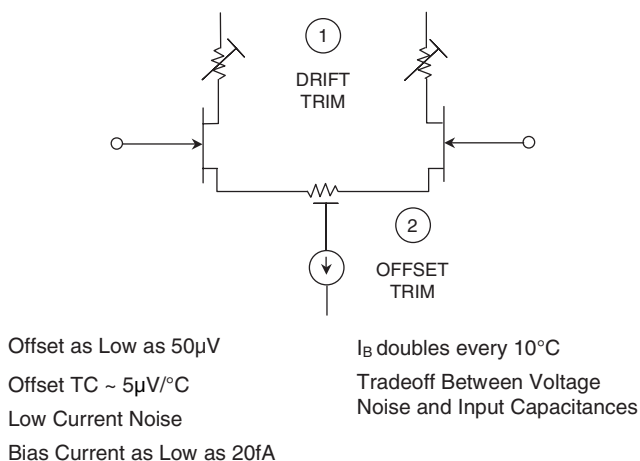
**Figure 1-25: The OP97, OP297 and OP497 op amp series uses superbeta input stage transistors and bias current compensation**

## FET Input Stages

Field-Effect Transistors (FETs) have much higher input impedance than do bipolar junction transistors (BJTs) and would therefore seem to be ideal devices for op amp input stages. However, they cannot be manufactured on all bipolar IC processes, and when a process does allow their manufacture, they often have their own problems.

FETs have high input impedance, low bias current, and good high frequency performance. (In an op amp, the lower  $g_m$  of the FET devices allows higher tail currents, thereby increasing the maximum slew rate.) FETs also have much lower current noise.

On the other hand, the input offset voltage of FET long-tailed pairs is not as good as the offset of corresponding BJTs, and trimming for minimum offset does not simultaneously minimize drift. A separate trim is needed for drift, and as a result, offset and drift in a JFET op amp, while good, aren't as good as the best BJTs. A simplified trim procedure for an FET input op amp stage is shown in Figure 1-26.



**Figure 1-26: Junction field effect transistor (JFET) input op amp stage showing offset and drift trims**

It is possible to make JFET op amps with very low voltage noise, but the devices involved are very large and have quite high input capacitance, which varies with input voltage, and so a trade-off is involved between voltage noise and input capacitance.

The bias current of an FET op amp is the leakage current of the gate diffusion (or the leakage of the gate protection diode, which has similar characteristics for a MOSFET). Such leakage currents double with every  $10^\circ\text{C}$  increase in chip temperature so that a FET op amp bias current is *one thousand times greater* at  $125^\circ\text{C}$  than at  $25^\circ\text{C}$ . Obviously this can be important when choosing between a bipolar or FET input op amp, especially in high temperature applications where bipolar op amp input bias current actually decreases.

Thus far, we have spoken generally of all kinds of FETs, that is, junction (JFETs) and MOS (MOSFETs). In practice, combined bipolar/JFET technology op amps (i.e., BiFET) achieve better performance than op amps using purely MOSFET or CMOS technology. While ADI and others make high performance op amps with MOS or CMOS input stages, in general these op amps have worse offset and drift, voltage noise, high-frequency performance than the bipolar counterparts. The power consumption is usually somewhat lower than that of bipolar op amps with comparable, or even better, performance.

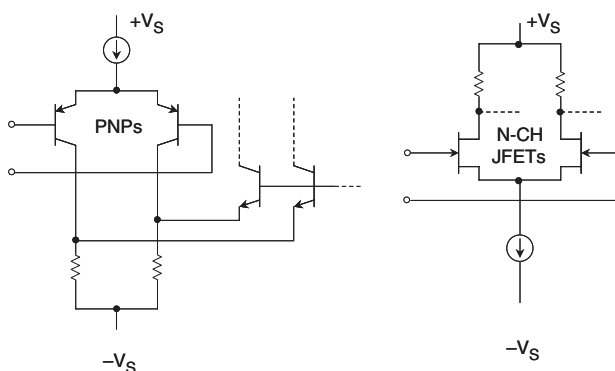
JFET devices require more headroom than do BJTs, since their pinch-off voltage is typically greater than a BJTs base-emitter voltage. Consequently, they are more difficult to operate at very low power supply voltages (1–2 V). In this respect, CMOS has the advantage of requiring less headroom than JFETs.



## Rail-Rail Input Stages

Today, there is common demand for op amps with input CM voltage that includes *both* supply rails, i.e., *rail-to-rail* CM operation. While such a feature is undoubtedly useful in some applications, engineers should recognize that there are still relatively few applications where it is absolutely essential. These applications should be distinguished from the many more applications where a CM range *close* to the supplies, or one that includes *one* supply, is necessary, but true input rail-to-rail operation is not.

In many single-supply applications, it is required that the input CM voltage range extend to one of the supply rails (usually ground). High side or low side current-sensing applications are examples of this. Many amplifiers can handle 0 V CM inputs, and they are easily designed using PNP differential pairs (or N-channel JFET pairs) as shown in Figure 1-27. The input CM range of such an op amp generally extends from about 200 mV below the negative rail ( $-V_S$  or ground), to about 1 V–2 V of the positive rail,  $+V_S$ .



**Figure 1-27: PNP or N-channel JFET stages allow CM inputs to the negative rail**

An input stage could also be designed with NPN transistors (or P-channel JFETs), in which case the input CM range would include the positive rail, and go to within about 1 V–2 V of the negative rail. This requirement typically occurs in applications such as high-side current sensing. The OP282/OP482 input stage uses a P-channel JFET input pair whose input CM range includes the positive rail, making it suitable for high-side sensing.

The AD823 is a dual 16 MHz ( $G = +1$ ) op amp with an N-channel JFET input stage (as in Figure 1-27). A simplified schematic of the AD823 is shown in Figure 1-28. This device can operate on single-supply voltages from +3 V to +36 V. This range also allows operation on traditional  $\pm 5$  V, or  $\pm 15$  V dual supplies if desired. Similar devices in a related (but lower power) family include the AD820, the AD822, and the AD824.

The AD823 JFET input stage allows the input common-mode voltage to range from 200 mV below the negative supply to within about 1.5 V of the positive supply. Input offset voltage is 0.8 mV maximum at 25°C, input bias current is 25 pA maximum at 25°C, offset voltage drift is 2  $\mu\text{V}/^\circ\text{C}$ , and input voltage noise is 16  $\text{nV}/\sqrt{\text{Hz}}$ . Current noise is only 1  $\text{fA}/\sqrt{\text{Hz}}$ . The AD823 is laser wafer trimmed for both offset voltage and offset voltage drift as described above.

A simplified diagram of a true rail-to-rail input stage is shown in Figure 1-29. Note that this requires use of *two* long-tailed pairs: one of PNP bipolar transistors Q1–Q2, the other of NPN transistors Q3–Q4. Similar input stages can also be made with CMOS pairs.

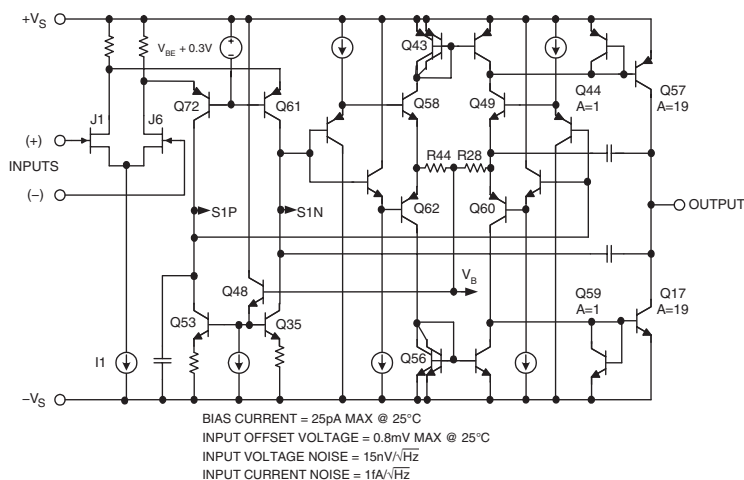


Figure 1-28: AD823 JFET input op amp simplified schematic

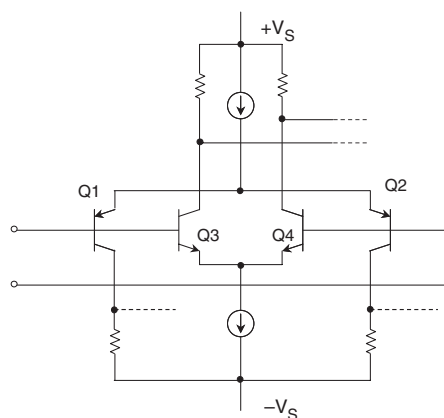


Figure 1-29: A true rail-to-rail bipolar transistor input stage

It should be noted that these two pairs will exhibit *different* offsets and bias currents, so when the applied CM voltage changes, the amplifier input offset voltage and input bias current does also. In fact, when both current sources remain active throughout most of the entire input common-mode range, amplifier input offset voltage is the *average* offset voltage of the two pairs. In those designs where the current sources are alternatively switched off at some point along the input common-mode voltage, amplifier input offset voltage is dominated by the PNP pair offset voltage for signals near the negative supply, and by the NPN pair offset voltage for signals near the positive supply. As noted, a true rail-to-rail input stage can also be constructed from CMOS transistors, for example as in the case of the CMOS AD8531/AD8532/AD8534 op amp family.

Amplifier input bias current, a function of transistor current gain, is also a function of the applied input common-mode voltage. The result is relatively poor common-mode rejection (CMR), and a changing common-mode input impedance over the CM input voltage range, compared to familiar dual-supply devices. These specifications should be considered carefully when choosing a rail-to-rail input op amp, especially

for a noninverting configuration. Input offset voltage, input bias current, and even CMR may be quite good over *part* of the common-mode range, but much worse in the region where operation shifts between the NPN and PNP devices, and vice versa.

True rail-to-rail amplifier input stage designs must transition from one differential pair to the other differential pair, somewhere along the input CM voltage range. Some devices like the OP191/OP291/OP491 family and the OP279 have a common-mode crossover threshold at approximately 1 V below the positive supply (where signals do not often occur). The PNP differential input stage is active from about 200mV below the negative supply to within about 1 V of the positive supply. Over this common-mode range, amplifier input offset voltage, input bias current, CMR, input noise voltage/current are primarily determined by the characteristics of the PNP differential pair. At the crossover threshold, however, amplifier input offset voltage becomes the average offset voltage of the NPN/PNP pairs and can change rapidly.

Also, as noted previously, amplifier bias currents are dominated by the PNP differential pair over most of the input common-mode range, and change polarity and magnitude at the crossover threshold when the NPN differential pair becomes active.

Op amps like the OP184/OP284/OP484 family, shown in Figure 1-30, utilize a rail-to-rail input stage design where both NPN and PNP transistor pairs are active throughout most of the entire input CM voltage range. With this approach to biasing, there is no CM crossover threshold. Amplifier input offset voltage is the average offset voltage of the NPN and the PNP stages, and offset voltage exhibits a smooth transition throughout the entire input CM range, due to careful laser trimming of input stage resistors.

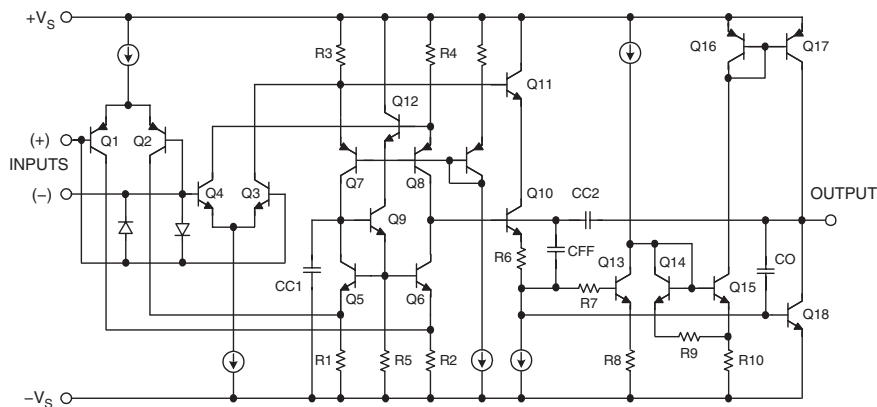


Figure 1-30: OP284 op amp simplified schematic shows true rail-to-rail input stage

In the same manner, through careful input stage current balancing and input transistor design, the OP184 family input bias currents also exhibit a smooth transition throughout the entire CM input voltage range. The exception occurs at the very extremes of the input range, where amplifier offset voltages and bias currents increase sharply, due to the slight forward-biasing of parasitic p-n junctions. This occurs for input voltages within approximately 1 V of either supply rail.

When *both* differential pairs are active throughout most of the entire input common-mode range, amplifier transient response is faster through the middle of the common-mode range by as much as a factor of 2 for bipolar input stages and by a factor of  $\sqrt{2}$  for JFET input stages. This is due to the higher transconductance of two operating input stages.

Input stage  $g_m$  determines the slew rate and the unity-gain crossover frequency of the amplifier, hence response time degrades slightly at the extremes of the input common-mode range when either the PNP stage (signals approaching the positive supply rail) or the NPN stage (signals approaching the negative supply rail) are forced into cutoff. The thresholds at which the transconductance changes occur are approximately within 1 V of either supply rail, and the behavior is similar to that of the input bias currents.

In light of the many quirks of true rail-to-rail op amp input stages, applications that do require true rail-to-rail inputs should be carefully evaluated, and an amplifier chosen to ensure that its input offset voltage, input bias current, common-mode rejection, and noise (voltage and current) are suitable.

### Don't Forget Input Overvoltage Considerations

In order to achieve the performance levels required, it is sometimes not possible to provide complete overdrive protection within IC op amps. Although most op amps have some type of input protection, care must still be taken to prevent possible damage against both CM and differential voltage stress.

This is most likely to occur, for example, when the input signal comes from an external sensor. Rather than present a cursory discussion of this topic here, the reader is instead referred to Chapter 7, Section 7-4 for a detailed examination of this important issue.

### Output Stages

The earliest IC op amp output stages were NPN emitter followers with NPN current sources or resistive pull-downs, as shown in Figure 1-31A. Naturally, the slew rates were greater for positive-going than they were for negative-going signals.

While all modern op amps have push-pull output stages of some sort, many are still asymmetrical, and have a greater slew rate in one direction than the other. Asymmetry tends to introduce distortion on ac signals and generally results from the use of IC processes with faster NPN than PNP transistors. It may also result in an ability of the output to approach one supply more closely than the other in terms of saturation voltage.

In many applications, the output is required to swing only to one rail, usually the negative rail (i.e., ground in single-supply systems). A pull-down resistor to the negative rail will allow the output to approach that rail (provided the load impedance is high enough, or is also grounded to that rail), but only slowly. Using an FET current source instead of a resistor can speed things up, but this adds complexity, as shown in Figure 1-31B.

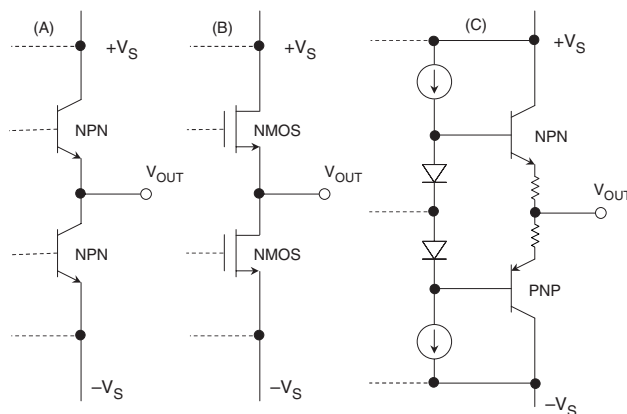


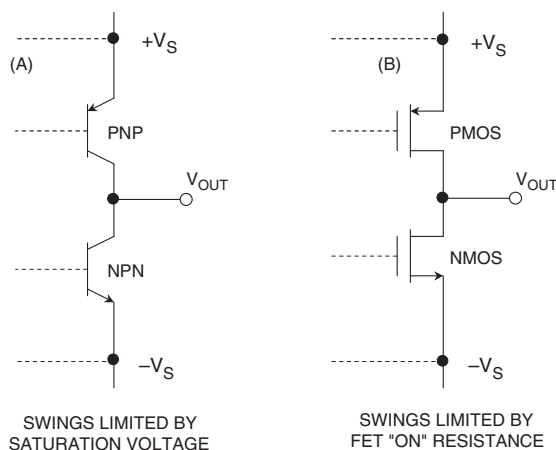
Figure 1-31: Some traditional op amp output stages

With modern complementary bipolar (CB) processes, well matched high speed PNP and NPN transistors are readily available. The complementary emitter follower output stage shown in Figure 1-31C has many advantages, but the most outstanding one is the low output impedance. However, the output voltage of this stage can only swing within about one  $V_{BE}$  drop of either rail. Therefore an output swing of 1 V to 4 V is typical of such a stage, when operated on a single 5 V supply.

The complementary common-emitter/common-source output stages shown in Figure 1-32A and B allow the op amp output voltage to swing much closer to the rails, but these stages have much higher open-loop output impedance than do the emitter follower-based stages of Figure 1-31C.

In practice, however, the amplifier's high open-loop gain and the applied feedback can still produce an application with low output impedance (particularly at frequencies below 10 Hz). What should be carefully evaluated with this type of output stage is the loop gain within the application, with the load in place. Typically, the op amp will be specified for a minimum gain with a load resistance of 10 k $\Omega$  (or more). Care should be taken that the application loading doesn't drop lower than the rated load, or gain accuracy may be lost.

It should also be noted these output stages can cause the op amp to be more sensitive to capacitive loading than the emitter-follower type. Again, this will be noted on the device data sheet, which will indicate a maximum of capacitive loading before overshoot or instability will be noted.



**Figure 1-32: "Almost" rail-to-rail output structures**

The complementary common emitter output stage using BJTs (Figure 1-32A) cannot swing completely to the rails, but only to within the transistor saturation voltage ( $V_{CESAT}$ ) of the rails. For small amounts of load current (less than 100  $\mu$ A), the saturation voltage may be as low as 5 mV to 10 mV, but for higher load currents, the saturation voltage can increase to several hundred mV (for example, 500 mV at 50 mA).

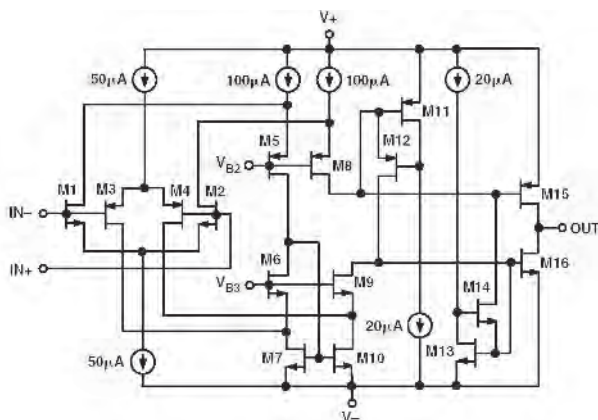
On the other hand, an output stage constructed of CMOS FETs (Figure 1-32B) can provide nearly true rail-to-rail performance, but only under no-load conditions. If the op amp output must source or sink substantial current, the output voltage swing will be reduced by the  $I \times R$  drop across the FETs internal "on" resistance. Typically this resistance will be on the order of 100  $\Omega$  for precision amplifiers, but it can be less than 10  $\Omega$  for high current drive CMOS amplifiers.

For the above basic reasons, it should be apparent that there is no such thing as a *true* rail-to-rail output stage, hence the caption of Figure 1-32 (“Almost” Rail-to-Rail Output Structures). The best any op amp output stage can do is an almost rail-to-rail swing, when it is lightly loaded.

Op amps built on foundry CMOS processes have a primary advantage of low cost. Also, it is relatively straightforward to design rail-to-rail input and output stages with these CMOS devices, which will operate on low supply voltages.

Figure 1-33 shows a simplified schematic of the AD8531/AD8532/AD8534 (single/dual/quad) op amp, which is typical of these design types. The AD8531/AD8532/AD8534 operates on a single 2.7 V to 6.0 V supply and can drive 250 mA. Input offset voltage is 25 mV maximum at 25°C, and voltage noise 45 nV/ $\sqrt{\text{Hz}}$ .

This type of op amp is simple and cost effective, and the lack of high dc precision is often no disadvantage. To the contrary, the high output drive available can be an overriding plus, particularly in AC-coupled applications.



**Figure 1-33: AD8531/AD8532/AD8534 CMOS rail-to-rail op amp simplified schematic**

### Output Stage Surge Protection

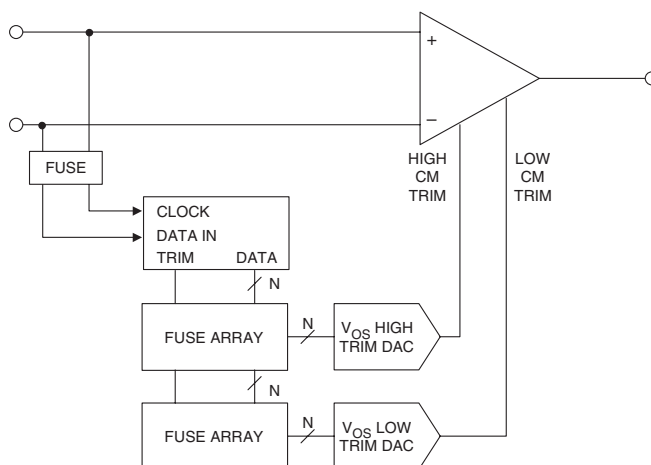
Most low speed, high precision op amps generally have output stages which are protected against short circuits to ground or to either supply. Their output current is limited to a little more than 10 mA. This has the additional advantage of minimizing self-heating of the chip (and thus minimizing dc errors due to chip temperature differentials).

If an op amp is required to deliver both high precision and a large output current, it is advisable to use a separate output stage (within the loop) to minimize self-heating of the precision op amp. A simple buffer amplifier such as the BUF04, or a section of a nonprecision op amp can be used.

Note that high speed op amps cannot have output currents limited to low values, as it would affect their slew rate and load drive ability. Thus most high speed op amps will source/sink between 50 mA–100 mA. Although many high speed op amps have internal protection for *momentary* shorts, their junction temperatures can be exceeded with sustained shorts. The user needs to be wary, and consult the specific device ratings.

## Offset Voltage Trim Processes

The AD860x CMOS op amp family exploits the advantages of digital technology to minimize the offset voltage normally associated with CMOS amplifiers. Offset voltage trimming is done after the devices are packaged. A digital code is entered into the device to adjust the offset voltage to less than 1 mV, depending upon the grade. Wafer testing is not required, and the patented ADI technique called DigiTrim™ requires no extra pins to accomplish the function. These devices have rail-to-rail inputs and outputs (similar to Figure 1-33), and the NMOS and PMOS parallel input stages are trimmed separately using DigiTrim to minimize the offset voltage in both pairs. A functional diagram of the AD8602 DigiTrim op amp is shown in Figure 1-34.



**Figure 1-34: AD8602 (1/2) CMOS op amp showing DigiTrim**

DigiTrim adjusts the offset voltage by programming digitally weighted current sources. The trim information is entered through existing pins using a special digital sequence. The adjustment values can be temporarily programmed, evaluated, and readjusted for optimum accuracy before permanent adjustment is performed. After the trim is completed, the trim circuit is locked out to prevent the possibility of any accidental re-trimming by the end user.

The physical trimming, achieved by blowing polysilicon fuses, is very reliable. No extra pads or pins are required, and no special test equipment is needed to perform the trimming. The trims can be done after packaging so that assembly-related shifts can be eliminated. No testing is required at the wafer level because of high die yields

The first devices to use this new technique are the Analog Devices' AD8601/02/04 (single, dual, quad) rail-to-rail CMOS amplifiers. The offset is trimmed for both high and low common-mode conditions so that the offset voltage is under 500  $\mu\text{V}$  over the full common-mode input voltage range. The bandwidth of the op amps is 8 MHz, slew rate is 5 V/ $\mu\text{s}$ , and supply current is only 640  $\mu\text{A}$  per amplifier.

At this point it is useful to review the other popular trim methods. Analog Devices pioneered the use of thin film resistors and laser wafer trimming for precision amplifiers, references, data converters, and other linear ICs (see Reference 5). Up to 16-bit accuracy can be achieved with trimming, and the thin film resistors themselves are very stable with temperature and can add to the thermal stability and accuracy of

a device, even without trimming. Thin film deposition and patterning are processes that must be tightly controlled. The laser trimming systems are also quite expensive. In-package trimming is not possible, so assembly-related shifts cannot be easily compensated. Nevertheless, thin film trimming at the wafer level provides continuous fine trim resolution in precision integrated circuits where high accuracy and stability are required.

*Zener zapping* uses a voltage to create a metallic short circuit across the base-emitter junction of a transistor to remove a circuit element (see References 4 and 6). The base-emitter junction is commonly referred to as a zener, although the mechanism is actually avalanche breakdown of the junction. During the avalanche breakdown across the base-emitter junction, the very high current densities and localized heating generate rapid metal migration between the base and emitter connections, leading to a metallic short across the junction. With proper biasing (current, voltage, and time), this short will have a very low resistance value. If a series of these base-emitter junctions are arranged in parallel with a string of resistors, zapping selected junctions will short out portions of the resistor string, thereby adjusting the total resistance value.

It is possible to perform zener zap trimming in the packaged IC to compensate for assembly-related shifts in the offset voltage. However, trimming in the package requires extra package pins. Alternately, trimming at the wafer level requires additional probe pads. Probe pads do not scale effectively as the process features shrink. Thus, the die area required for trimming is relatively constant, regardless of the process geometries. Some form of bipolar transistor is required for the trim structures, therefore a purely MOS-based process may not have zener zap capability. The nature of the trims is discrete since each zap removes a predefined resistance value. Increasing trim resolution requires additional transistors and pads or pins, which rapidly increase the total die area and/or package cost. This technique is most cost-effective for fairly large geometry processes where the trim structures and probe pads make up a relatively small percentage of the overall die area.

It was in the process of creating the industry standard OP07 in 1975 that Precision Monolithics Incorporated pioneered zener zap trimming (Reference 6). The OP07 and other similar parts must be able to operate from over  $\pm 15$  V supplies. As a result, they utilize relatively large device geometries to support the high voltage requirements, and extra probe pads don't significantly increase die area.

*Link trimming* is the cutting of metal or poly-silicon links to remove a connection. In link trimming, either a laser or a high current is used to destroy a "shorted" connection across a parallel resistive element. Removing the connection increases the effective resistance of the combined element(s). Laser cutting is similar to laser trimming of thin films. The high local heat from the laser beam causes material changes that lead to a nonconductive area, effectively cutting a metal or conductive polysilicon connector.

The high-current link trim method works as an inverse to zener zapping—the conductive connection is destroyed, rather than created by a zener-zap.

Link trim structures tend to be somewhat more compact than laser trimmed resistor structures. No special processes are required in general, although the process may have to be tailored to the laser characteristics if laser cutting is used. With the high-current trimming method, testing at the wafer level may not be required if die yields are good. The laser cutting scheme doesn't require extra contact pads, but the trim structures don't scale with the process feature sizes. Laser cutting of links cannot be performed in the package, and requires additional probe pads on the die. In addition, it can require extra package pins for in-package high-current trims. Like zener zapping, link trimming is discrete. Resolution improvements require additional structures, increasing area and cost.

*EEPROM trimming* utilizes special, nonvolatile digital memory to store trim data. The stored data bits control adjustment currents through on-chip D/A converters. Memory cells and D/A converters scale with



the process feature size. In-package trimming and even trimming in the customer's system is possible so that assembly-related shifts can be trimmed out. Testing at the wafer level is not required if yields are reasonable. No special hardware is required for the trimming beyond the normal mixed-signal tester system, although test software development may be more complicated.

Since the trims can be overwritten, it is possible to periodically reprogram the system to account for long-term drifts or to modify system characteristics for new requirements. The number of reprogram cycles possible depends on the process, and is finite. Most EEPROM processes provide enough rewrite cycles to handle routine recalibration.

This trim method does require special processing. Stored trim data can be lost under certain conditions, especially at high operating temperatures. At least one extra digital contact pad/package pin is required to input the trim data to the on-chip memory.

This technique is only available on MOS-based processes due to the very thin oxide requirements. The biggest drawback is that the on-chip D/A converters are large—often larger than the amplifier circuits they are adjusting. For this reason, EEPROM trimming is mostly used for data converter or system-level products where the trim D/A converters represent a much smaller percentage of the overall die area.

Figure 1-35 summarizes the key features of each ADI trim method. It can be seen from that all trim methods have their respective places in producing high performance linear integrated circuits.

PROCESS	TRIMMED AT:	SPECIAL PROCESSING	RESOLUTION
DigiTrim™	Wafer or Final Test	None	Discrete
Laser Trim	Wafer	Thin Film Resistor	Continuous
Zener Zap Trim	Wafer	None	Discrete
Link Trim	Wafer	Thin Film or Poly Resistor	Discrete
EEPROM Trim	Wafer or Final Test	EEPROM	Discrete

Figure 1-35: Summary of ADI trim processes

## Op Amp Process Technologies

The wide variety of op amp processes is shown in Figure 1-36. The early 1960s op amps used standard NPN-based bipolar processes. The PNP transistors of these processes were extremely slow and were used primarily for current sources and level-shifting.

The ability to produce matching high speed PNP transistors on a bipolar process added great flexibility to op amp circuit designs. The first p-epi complementary bipolar (CB) process was introduced by ADI in the mid-1980s. The  $f_t$ s of the PNP and NPN transistors were approximately 700 MHz and 900 MHz, respectively, and had 30 V breakdowns. Since its original introduction in 1985, several additional CB processes have been developed at ADI designed for higher speeds and lower breakdowns. For example, a current 5 V CB process has 9 GHz PNPs and 16 GHz NPNs. These CB processes are used in today's precision op amps, as well as those requiring wide bandwidths.

- BIPOLAR (NPN-BASED): This is Where it All Started
- COMPLEMENTARY BIPOLAR (CB): Rail-to-Rail, Precision, High Speed
- BIPOLAR + JFET (BiFET): High Input Impedance, High Speed
- COMPLEMENTARY BIPOLAR + JFET (CBFET): High Input Impedance, Rail-to-Rail Output, High Speed
- COMPLEMENTARY MOSFET (CMOS): Low Cost Op Amps  
(ADI DigiTrim Minimizes Offset Voltage and Drift in CMOS Op Amps)
- BIPOLAR (NPN) + CMOS (BiCMOS): Bipolar Input Stage adds Linearity, Low Power, Rail-to-Rail Output
- COMPLEMENTARY BIPOLAR + CMOS (CBCMOS): Rail-to-Rail Inputs, Rail-to-Rail Outputs, Good Linearity, Low Power, Higher Cost

**Figure 1-36: Op amp process technology summary**

The JFETs available on the Analog Devices complementary bipolar processes allow high input impedance op amps to be designed suitable for such applications as photodiode or electrometer preamplifiers. These processes are sometimes designated as *CBFET*.

CMOS op amps, generally have higher offset voltages and offset voltage drift than trimmed bipolar or BiFET op amps, however the Analog Devices DigiTrim process described above yields low offset voltage, while keeping costs low. Voltage noise for CMOS op amps tends to be larger, but the input bias current is very low. They offer low power and cost (foundry CMOS processes are typically used).

The addition of bipolar or complementary devices to a CMOS process (BiMOS or CBCMOS) adds greater flexibility, better linearity, and lower power as well as additional cost. The bipolar devices are typically used for the input stage to provide good gain and linearity, and CMOS devices for the rail-to-rail output stage.

In summary, there is no single IC process that is optimum for all op amps. Process selection and the resulting op amp design depends on the targeted applications and ultimately should be transparent to the customer.

## References: Op Amp Structures

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2. George Erdi, “Amplifier Techniques for Combining Low Noise, Precision, and High-Speed Performance,” **IEEE Journal of Solid-State Circuits**, Vol. SC-16, December, 1981 pp. 653–661.
3. George Erdi, Tom Schwartz, Scott Bernardi, and Walt Jung, “Op Amps Tackle Noise and for Once, Noise Loses,” **Electronic Design**, December 12, 1980.
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5. Richard Wagner, “Laser-Trimming on the Wafer,” **Analog Dialogue**, Vol. 9, No. 3, pp. 3–5.
6. Donn Soderquist, George Erdi, “The OP07 UltraLow Offset Voltage Op Amp,” **Precision Monolithics AN-13**, December, 1975.
7. Walt Kester, Editor, **Linear Design Seminar**, Analog Devices, 1995, ISBN: 0-916550-15-X.
8. Walt Kester, Editor, **High Speed Design Techniques**, Analog Devices, 1996, ISBN: 0-916550-17-6 (available for download at [www.analog.com](http://www.analog.com)).
9. Walt Kester, Editor, **Practical Analog Design Techniques**, Analog Devices, 1995, ISBN: 0-916550-16-8. (available for download at [www.analog.com](http://www.analog.com)).

## Op Amp Specifications

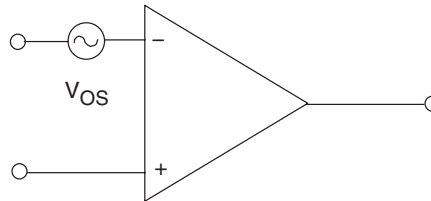
*Walt Kester, Walt Jung, James Bryant*

Most op amp specifications are largely topology independent. However, although voltage feedback and current feedback op amps have similar error terms and specifications, the application of each part warrants discussing some of the specifications separately. In the following discussions, this will be done where significant differences exist.

### Input Offset Voltage, $V_{OS}$

Ideally, if both inputs of an op amp are at exactly the same voltage, the output should be at zero volts. In practice, a small differential voltage must be applied to the inputs to force the output to zero. This is known as the *input offset voltage*,  $V_{OS}$ .

Input offset voltage is modeled as a voltage source,  $V_{OS}$ , in series with the inverting input terminal of the op amp as shown in Figure 1-37. The corresponding output offset voltage (due to  $V_{OS}$ ) is obtained by multiplying the input offset voltage by the dc noise gain of the circuit (see Figure 1-3 and Eq. 1-2).



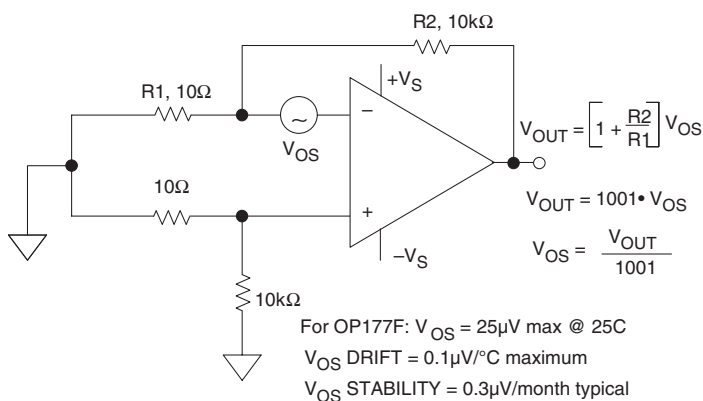
- Offset Voltage: The differential voltage that must be applied to the input of an op amp to produce zero output.
- Ranges:
  - Chopper-Stabilized Op Amps:  $<1\mu\text{V}$
  - General-Purpose Precision Op Amps:  $50\text{--}500\mu\text{V}$
  - Best Bipolar Op Amps:  $10\text{--}25\mu\text{V}$
  - Best FET Op Amps:  $100\text{--}1,000\mu\text{V}$
  - High Speed Op Amps:  $100\text{--}2,000\mu\text{V}$
  - Untrimmed CMOS Op Amps:  $5,000\text{--}50,000\mu\text{V}$
  - DigiTrim CMOS Op Amps:  $<1,000\mu\text{V}$

**Figure 1-37: Input offset voltage**

Chopper stabilized op amps have a  $V_{OS}$  that is less than  $1\mu\text{V}$  (AD8551 series), and the best precision bipolar op amps (super-beta or bias stabilized) can have offsets as low as  $25\mu\text{V}$  (OP177F). The very best trimmed FET types have about  $100\mu\text{V}$  of offset (AD8610B), and untrimmed CMOS op amps can range from  $5\text{ mV}$  to  $50\text{ mV}$ . However, the ADI DigiTrim CMOS op amps have offset voltages less than  $1\text{ mV}$  (AD8605). Generally speaking, “precision” op amps will have  $V_{OS} < 0.5\text{ mV}$ , although some high speed amplifiers may be a little worse than this.

Measuring input offset voltages of a few microvolts requires that the test circuit does not introduce more error than the offset voltage itself. Figure 1-38 shows a standard circuit for measuring offset voltage. The circuit amplifies the input offset voltage by the noise gain of 1001. The measurement is made at the amplifier output using an accurate digital voltmeter. The offset referred to the input (RTI) is calculated by dividing the output voltage by the noise gain. The small source resistance seen by the inputs results in negligible bias current contribution to the measured offset voltage. For example, 2 nA bias current flowing through the 10  $\Omega$  resistor produces a 0.02  $\mu$ V error referred to the input.

As simple as this circuit looks, it can give inaccurate results when testing precision op amps, unless care is taken in implementation. The largest potential error source comes from parasitic thermocouple junctions, formed where two different metals are joined. This thermocouple voltage can range from 2  $\mu$ V/ $^{\circ}$ C to more than 40  $\mu$ V/ $^{\circ}$ C. Note that in this circuit additional “dummy” resistors have been added to the noninverting input, in order to exactly match/balance the thermocouple junctions in the inverting input path.



**Figure 1-38: Measuring input offset voltage**

The accuracy of the measurement also depends on the mechanical layout of the components and exactly how they are placed on the PC board. Keep in mind that the two connections of a component such as a resistor create two equal, but opposite polarity thermoelectric voltages (assuming they are connected to the same metal, such as the copper trace on a PC board). These will cancel each other, *assuming both are at exactly the same temperature*. Clean connections and short lead lengths help to minimize temperature gradients and increase the accuracy of the measurement. Note—see the Chapter 7 discussions on this general topic for more detail.

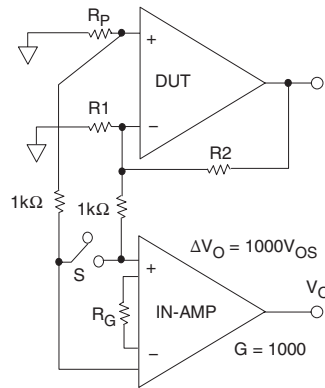
In the test circuit, airflow should be minimal so that all the thermocouple junctions stabilize at the same temperature. In some cases, the circuit should be placed in a small closed container to eliminate the effects of external air currents. The circuit should be placed flat on a surface so that convection currents flow up and off the top of the board, not across the components, as would be the case if the board were mounted vertically.

Measuring the offset voltage shift over temperature is an even more demanding challenge. Placing the printed circuit board containing the amplifier being tested in a small box or plastic bag with foam insulation prevents the temperature chamber air current from causing thermal gradients across the parasitic thermocouples. If cold testing is required, a dry nitrogen purge is recommended. Localized temperature cycling of the amplifier itself using a Thermostream-type heater/cooler may be an alternative, but these units tend to generate quite a bit of airflow that can be troublesome.

Generally, the test circuit of Figure 1-38 can be made to work for many amplifiers. Low absolute values for the small resistors (such as  $10\ \Omega$ ) will minimize bias current induced errors. An alternate  $V_{OS}$  measurement method is shown in Figure 1-39, and is suitable for cases of high and/or unequal bias currents (as in the case of current feedback op amps).

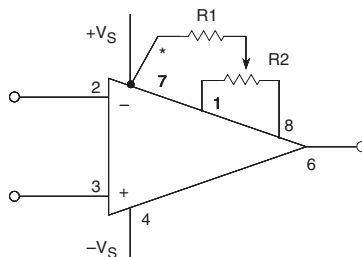
In this measurement method, an in amp is connected to the op amp input terminals through isolation resistors, and provides the gain for the measurement. The offset voltage of the in amp (measured with S closed) must then be subtracted from the final  $V_{OS}$  measurement. Also, the circuit shown in Figure 1-44, for measuring input bias currents, can also be used to measure input offset voltage independent of bias currents.

**Figure 1-39: Alternate input offset voltage measurement using an in amp**



### Offset Adjustment (Internal Method)

Many single op amps have pins available for optional offset null. To make use of this feature, two pins are joined by a potentiometer, and the wiper goes to one of the supplies through a resistor, as shown generally in Figure 1-40. Note that if the wiper is accidentally connected to the wrong supply, the op amp will probably be destroyed—this is a common problem, when one op amp type is replaced by another. The range of offset adjustment in a well-designed op amp is no more than two or three times the maximum  $V_{OS}$  of the



- \* Wiper connection may be to either  $+V_S$  or  $-V_S$  depending on op amp
- R values depend on op amp. Consult data sheet
- Use to null out input offset voltage, not system offsets
- There may be high gain from offset pins to output — Keep them quiet
- Nulling offset causes increase in offset temperature coefficient, approximately  $4\mu\text{V}/^\circ\text{C}$  for 1mV offset null for FET inputs

**Figure 1-40: Offset adjustment pins**

lowest grade device, in order to minimize sensitivity. Nevertheless, the voltage gain of an op amp at its offset adjustment pins may actually be greater than the gain at its signal inputs. It is therefore very important to keep these pins noise free. Note that it is *never* advisable to use long leads from an op amp to a remote nulling potentiometer.

As mentioned above, the offset drift of an op amp with temperature will vary with the setting of its offset adjustment. The internal adjustment terminals should therefore be used only to adjust the op amp's own offset, *not to correct any system offset errors*, since doing so would be at the expense of increased temperature drift. The drift penalty for a FET input op amp is on the order of  $4 \mu\text{V}/^\circ\text{C}$  for each millivolt of nulled offset voltage. It is generally better to control offset voltage by proper device/grade selection.

## Offset Adjustment (External Methods)

If an op amp doesn't have offset adjustment pins (popular duals and all quads do not), and it is still necessary to adjust the amplifier and system offsets, an external method can be used. This method is also most useful if the offset adjustment is to be done with a system programmable voltage, such as a DAC.

With an inverting op amp configuration, injecting current into the inverting input is the simplest method, as shown in Figure 1-41A. The disadvantage of this method is that some increase in noise gain is possible, due to the parallel path of  $R_3$  and the potentiometer resistance. The resulting increase in noise gain may be reduced by making  $\pm V_R$  large enough so that the  $R_3$  value is much greater than  $R_1 \parallel R_2$ . Note that if the power supplies are stable and noise free, they can be used as  $\pm V_R$ .

Figure 1-41B shows how to implement offset trim by injecting a small offset voltage into the noninverting input. This circuit is preferred over Figure 1-41A, as it results in no noise gain increase (but it requires adding  $R_p$ ). If the op amp has matched input bias currents,  $R_p$  should equal  $R_1 \parallel R_2$  (to minimize the added offset voltage). Otherwise,  $R_p$  should be less than  $50 \Omega$ . For higher values, it may be advisable to bypass  $R_p$  at high frequencies.

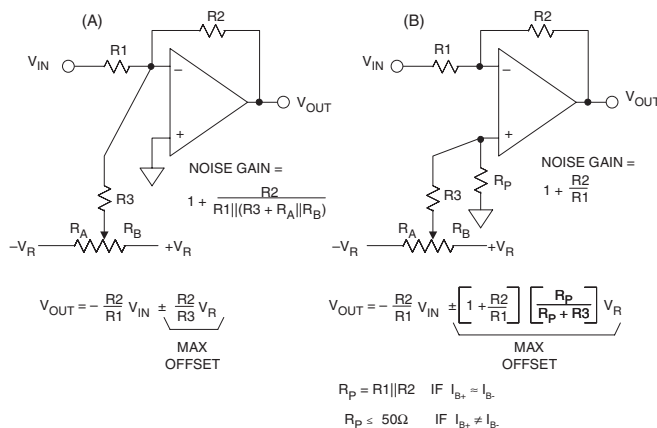
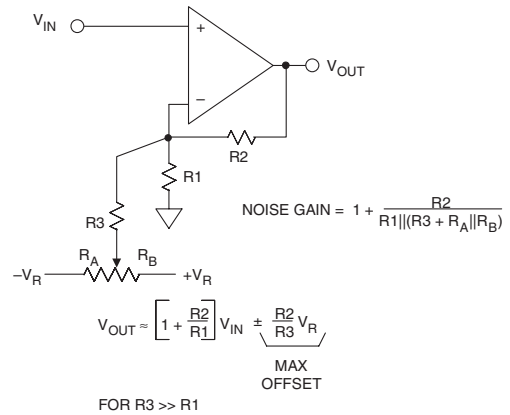


Figure 1-41: Inverting op amp external offset trim methods

The circuit shown in Figure 1-42 can be used to inject a small offset voltage when using an op amp in the noninverting mode. This circuit works well for small offsets, where  $R_3$  can be made much greater than  $R_1$ . Note that otherwise, the signal gain might be affected as the offset potentiometer is adjusted. The gain may be stabilized, however, if  $R_3$  is connected to a fixed low impedance reference voltage source,  $\pm V_R$ .

**Figure 1-42: Noninverting op amp external offset trim methods**



### Input Offset Voltage Drift and Aging Effects

Input offset voltage varies with temperature, and its temperature coefficient is known as  $TCV_{OS}$ , or more commonly, *drift*. As we have mentioned, offset drift is affected by offset adjustments to the op amp, but when it has been minimized, it may be as low as  $0.1 \mu\text{V}/^\circ\text{C}$  (typical value for OP177F). More typical drift values for a range of general purpose precision op amps lie in the range  $1\text{--}10 \mu\text{V}/^\circ\text{C}$ . Most op amps have a specified value of  $TCV_{OS}$ , but instead, some have a second value of maximum  $V_{OS}$  that is guaranteed over the operating temperature range. Such a specification is less useful, because there is no guarantee that  $TCV_{OS}$  is constant or monotonic.

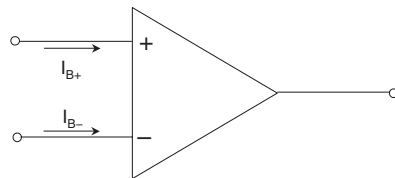
The offset voltage also changes as time passes, or *ages*. Aging is generally specified in  $\mu\text{V}/\text{month}$  or  $\mu\text{V}/1000$  hours, but this can be misleading. Since aging is a “drunkard’s walk” phenomenon it is proportional to the *square root* of the elapsed time. An aging rate of  $1 \mu\text{V}/1000$  hour therefore becomes about  $3 \mu\text{V}/\text{year}$  (not  $9 \mu\text{V}/\text{year}$ ).

*Long-term stability* of the OP177F is approximately  $0.3 \mu\text{V}/\text{month}$ . This refers to a time period *after* the first 30 days of operation. Excluding the initial hour of operation, changes in the offset voltage of these devices during the first 30 days of operation are typically less than  $2 \mu\text{V}$ .

### Input Bias Current, $I_B$

Ideally, no current flows into the input terminals of an op amp. In practice, there are always two *input bias currents*,  $I_{B+}$  and  $I_{B-}$  (see Figure 1-43).

**Figure 1-43: Op amp input bias current**



- A very variable parameter
- $I_B$  can vary from  $60 \text{ fA}$  (1 electron every  $3 \mu\text{s}$ ) to many  $\mu\text{A}$ , depending on the device.
- Some structures have well-matched  $I_B$ , others do not.
- Some structures'  $I_B$  varies little with temperature, but a FET op amp's  $I_B$  doubles with every  $10^\circ\text{C}$  rise in temperature.
- Some structures have  $I_B$  that may flow in either direction.



Values of  $I_B$  range from 60 fA (about one electron every three microseconds) in the AD549 electrometer, to tens of microamperes in some high speed op amps. Op amps with simple input structures using BJT or FET long-tailed pair have bias currents that flow in one direction. More complex input structures (bias-compensated and current feedback op amps) may have bias currents that are the difference between two or more internal current sources, and may flow in either direction.

Bias current is a problem to the op amp user because it flows in external impedances and produces voltages, which add to system errors. Consider a noninverting unity gain buffer driven from a source impedance of 1 M $\Omega$ . If  $I_B$  is 10 nA, it will introduce an additional 10 mV of error. This degree of error is not trivial in any system.

If the designer simply forgets about  $I_B$  and uses capacitive coupling, the circuit won't work—at all. Or, if  $I_B$  is low enough, it may work momentarily while the capacitor charges, giving even more misleading results. The moral here is not to neglect the effects of  $I_B$ , in any op amp circuit. The same admonition goes for in amp circuits.

Input bias current (or input offset voltage) may be measured using the test circuit of Figure 1-44. To measure  $I_B$ , a large resistance,  $R_S$ , is inserted in series with the input under test, creating an apparent additional offset voltage equal to  $I_B \times R_S$ . If the actual  $V_{OS}$  has previously been measured and recorded, the change in apparent  $V_{OS}$  due to the change in  $R_S$  can be determined, and  $I_B$  is then easily computed. This yields values for  $I_{B+}$  and  $I_{B-}$ . The rated value of  $I_B$  is the average of the two currents, or  $I_B = (I_{B-} + I_{B+})/2$ .

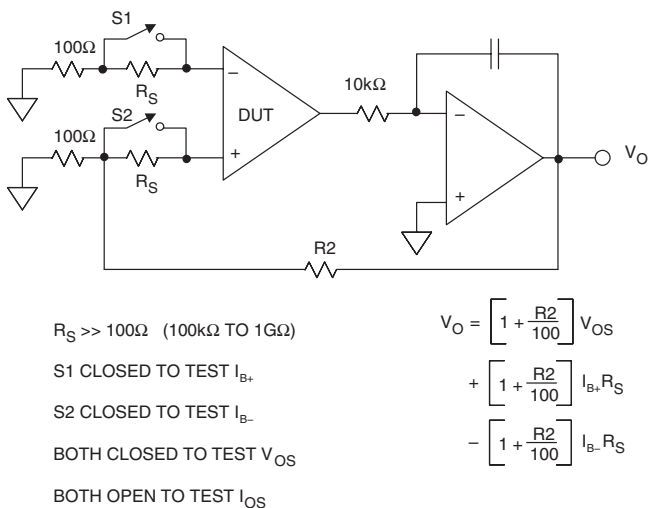


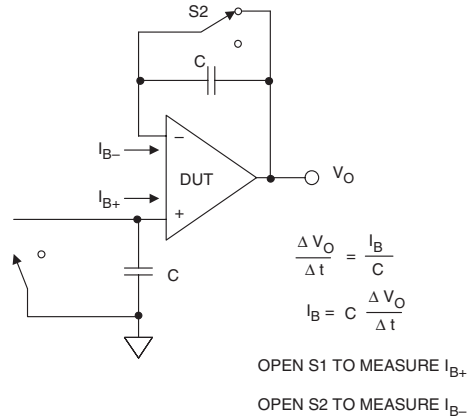
Figure 1-44: Measuring input bias current

The *input offset current*,  $I_{OS}$ , may also be calculated, by taking the difference between  $I_{B-}$  and  $I_{B+}$ , or  $I_{OS} = I_{B+} - I_{B-}$ . Typical useful  $R_S$  values vary from 100 k $\Omega$  for bipolar op amps to 1000 M $\Omega$  for some FET input devices.

Note also that  $I_{OS}$  is only meaningful where the two individual bias currents are fundamentally reasonably well-matched, to begin with. This is true for most VFB op amps. However, it wouldn't, for example, be meaningful to speak of  $I_{OS}$  for a CFB op amp, as the currents are radically unmatched.

Extremely low input bias currents must be measured by integration techniques. The bias current in question is used to charge a capacitor, and the rate of voltage change is measured. If the capacitor and general circuit leakage is negligible (this is very difficult for currents under 10 fA), the current may be calculated directly from the rate of change of the output of the test circuit. Figure 1-45 illustrates the general concept. With one switch open and the opposite closed, either  $I_{B+}$  or  $I_{B-}$  is measured.

**Figure 1-45: Measuring very low bias currents**



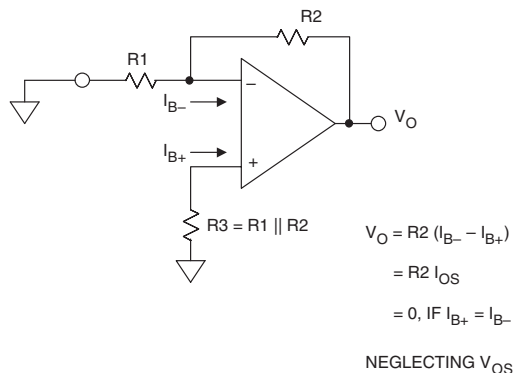
It should be obvious that only a premium capacitor dielectric can be used for C, for example Teflon or polypropylene types.

### Canceling the Effects of Bias Current (External to the Op Amp)

When the bias currents of an op amp are well matched (the case with simple bipolar op amps, but *not* internally bias compensated ones, as noted previously), a bias compensation resistor,  $R_3$ , ( $R_3 = R_1 \parallel R_2$ ) introduces a voltage drop in the noninverting input to match and thus compensate the drop in the parallel combination of  $R_1$  and  $R_2$  in the inverting input. This minimizes additional offset voltage error, as in Figure 1-46.

Note that if  $R_3$  is more than 1 k $\Omega$  or so, it should be bypassed with a capacitor to prevent noise pickup. Also note that this form of bias cancellation is useless where bias currents are not well-matched, and will, in fact, make matters worse.

**Figure 1-46: Canceling the effects of input bias current within an application**



## Calculating Total Output Offset Error Due to $I_B$ and $V_{OS}$

The equations shown in Figure 1-47 are useful in referring all the offset voltage and induced offset voltage from bias current errors to either the input (RTI) or the output (RTO) of the op amp. The choice of RTI or RTO is a matter of preference.

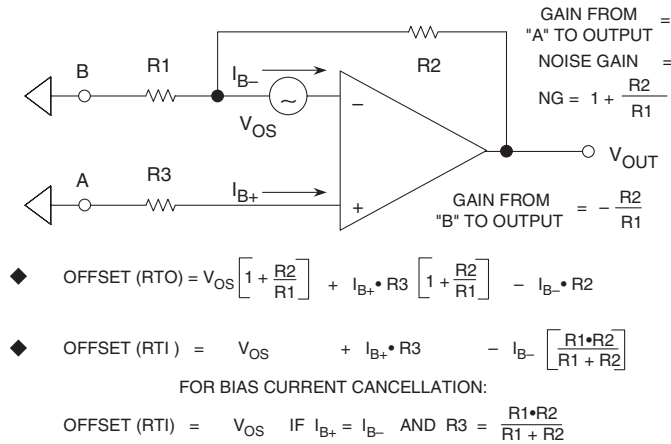


Figure 1-47: Op amp total offset voltage model

The RTI value is useful in comparing the cumulative op amp offset error to the input signal. The RTO value is more useful if the op amp drives additional circuitry, to compare the net errors with that of the next stage. In any case, the RTO value is obtained by multiplying the RTI value by the stage noise gain, which is  $1 + R_2/R_1$ .

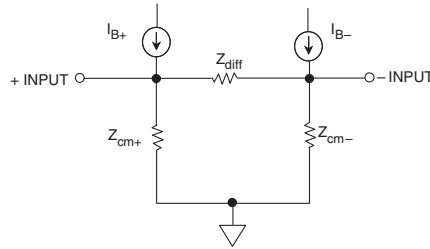
Before departing the topic of offset errors, some simple rules towards minimization might bear repetition:

- Keep input/feedback resistance values low, to minimize offset voltage due to bias current effects.
- Use a bias compensation resistance with VFB op amps *not* using internal bias compensation. Bypass this resistance, for lowest noise pickup.
- If a VFB op amp *does* use internal bias current compensation, *don't* use the compensation resistance.
- When necessary, use *external* offset trim networks, for lowest induced drift.
- Select an appropriate precision op amp specified for low offset and drift, as opposed to trimming.
- For high performance low drift circuitry, watch out for thermocouple effects and used balanced, low thermal error layouts.

## Input Impedance

VFB op amps normally have both differential and common-mode input impedances specified. Current feedback op amps normally specify the impedance to ground at each input. Different models may be used for different voltage feedback op amps, but in the absence of other information, it is usually safe to use the model in Figure 1-48. In this model, the bias currents flow into the inputs from infinite impedance current sources.

The common-mode input impedance data sheet specification ( $Z_{cm+}$  and  $Z_{cm-}$ ) is the impedance from either input to ground (NOT from both to ground). The differential input impedance ( $Z_{diff}$ ) is the impedance

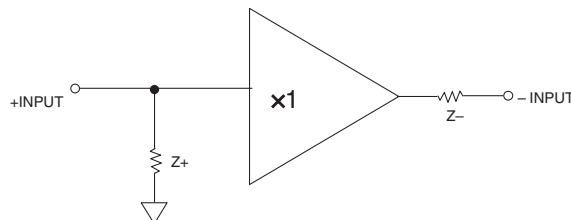


- $Z_{cm+}$  and  $Z_{cm-}$  are the common-mode input impedance. The figure on the data sheet is for one, not both, but they are approximately equal.  $Z_{diff}$  is the differential input impedance.
- They are high resistance ( $10^5 - 10^{12} \Omega$ ) in parallel with a small shunt capacitance (sometimes as high as 25pF).
- In most practical circuits,  $Z_{cm-}$  is swamped by negative feedback.

**Figure 1-48: Input impedance (voltage feedback op amp)**

between the two inputs. These impedances are usually resistive and high ( $10^5 \Omega$ – $10^{12} \Omega$ ) with some shunt capacitance (generally a few pF, sometimes 20 pF–25 pF). In most op amp circuits, the inverting input impedance is reduced to a very low value by negative feedback, and only  $Z_{cm+}$  and  $Z_{diff}$  are of importance.

A current feedback op amp is even more simple, as shown in Figure 1-49.  $Z_+$  is resistive, generally with some shunt capacitance, and high ( $10^5 \Omega$ – $10^9 \Omega$ ) while  $Z_-$  is reactive (L or C, depending on the device) but has a resistive component of  $10 \Omega$ – $100 \Omega$ , varying from type to type.

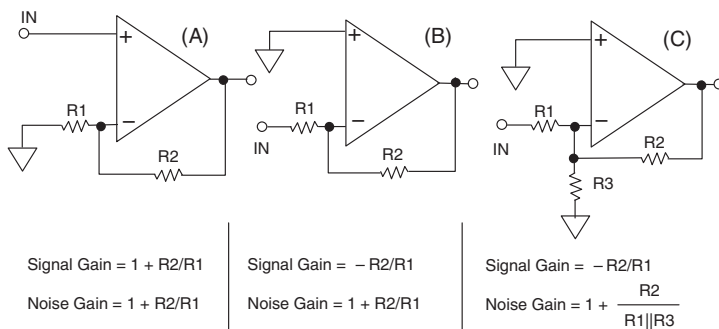


- $Z_+$  is high resistance ( $10^5 - 10^9 \Omega$ ) with little shunt capacitance.
- $Z_-$  is low and may be reactive (L or C). The resistive component is  $10$ – $100 \Omega$ .

**Figure 1-49: Input impedance (current feedback op amp)**

## Manipulating Op Amp Noise Gain and Signal Gain

Consider an op amp and two resistors, R1 and R2, arranged as shown in the series of figures of Figure 1-50. Note that R1 and R2 need not be resistors; they could also be complex impedances, Z1 and Z2.



- Voltage Noise and Offset Voltage of the op amp are reflected to the output by the Noise Gain.
- Noise Gain, not Signal Gain, is relevant in assessing stability.
- Circuit C has unchanged Signal Gain, but higher Noise Gain, thus better stability, worse noise, and higher output offset voltage.

**Figure 1-50: Manipulating op amp noise gain and signal gain**

If we ground R1 and apply a signal to the noninverting input, we see a signal gain of  $1 + R2/R1$ , as in Figure 1-50A. If we ground the noninverting input and apply the signal to R1, we see a signal gain of  $-R2/R1$ , as in Figure 1-50B. In both cases, the voltage noise of the op amp itself (as well as the input offset voltage) sees a gain of  $1 + R2/R1$ , i.e., the *noise gain* of the op amp, as discussed earlier in this chapter.

This discussion is aimed at making the point that a stage's noise gain and signal gain *need not necessarily be equal*. Some times it can be to the user's advantage to manipulate them, so as to be somewhat independent of one another.

But, importantly, *it is the noise gain that is relevant in assessing stability*. It is sometimes possible to alter the noise gain, while leaving signal gain unaffected. When this is done, a marginally stable op amp stage can sometimes be made stable, with the same signal gain.

For example, consider the inverting amplifier of Figure 1-50B. If we add a third resistor to Figure 1-50B, it becomes Figure 1-50C. This dummy resistor R3, from the inverting input to ground, increases the noise gain to  $1 + R2/(R1 \parallel R3)$ . But, note the signal gain is unaffected; that is it is still  $-R2/R1$ .

This provides a means of stabilizing an unstable inverting amplifier—at a cost of worse signal-to-noise ratio, less loop gain, and increased sensitivity to input offset voltage. Nevertheless, it is still a sometimes useful trick.

## Open-Loop Gain And Open-Loop Gain Nonlinearity

*Open-loop voltage gain*, usually called  $A_{VOL}$  (sometimes simply  $A_v$ ), for most VFB op amps is quite high. Common values are 100,000 to 1,000,000, and 10 or 100 times these figures for high precision parts.

Some fast op amps have appreciably lower open-loop gain, but gains of less than a few thousand are unsatisfactory for high accuracy use. Note also that open-loop gain isn't highly stable with temperature. It can vary quite widely from device to device of the same type, so it is important that it be reasonably high.

Since a voltage feedback op amp operates as voltage in/voltage out, its open-loop gain is a dimensionless ratio, so no unit is necessary. However, data sheets sometimes express gain in V/mV or V/ $\mu$ V instead of V/V, for the convenience of using smaller numbers. Or, voltage gain can also be expressed in dB terms, as gain in dB =  $20 \times \log A_{VOL}$ . Thus an open-loop gain of 1 V/ $\mu$ V is equivalent to 120 dB, and so on.

CFB op amps have a current input and a voltage output, so their open-loop *transimpedance gain* is expressed in volts per ampere or ohms (or k $\Omega$  or M $\Omega$ ). Values usually lie between hundreds of k $\Omega$  and tens of M $\Omega$ .

From basic feedback theory, it is understood that in order to maintain accuracy, a precision amplifier's dc open-loop gain,  $A_{VOL}$ , should be high. This can be seen by examining the closed-loop gain equation, including errors due to finite gain. The expression for closed loop gain with a finite gain error is:

$$G_{CL} = \frac{1}{\beta} \bullet \left[ \frac{1}{1 + \frac{1}{A_{VOL}\beta}} \right] \quad \text{Eq. 1-15A}$$

Since noise gain is equal to  $1/\beta$ , there are alternate forms of this expression. Combining the two right side terms and using the NG expression, an alternate one is:

$$G_{CL} = \frac{NG}{1 + \frac{NG}{A_{VOL}}} \quad \text{Eq. 1-15B}$$

Eqs. 1-15A and 1-15B are equivalent, and either can be used. As previously discussed, noise gain (NG) is simply the gain seen by a small voltage source in series with the op amp input, and is also the ideal amplifier signal gain in the noninverting mode. If  $A_{VOL}$  in Eqs. 1-15A and 1-15B is infinite, the closed-loop gain becomes exactly equal to the noise gain,  $1/\beta$ .

However, for  $NG \ll A_{VOL}$  and finite  $A_{VOL}$ , there is a closed-loop gain error estimation:

$$\text{Closed loop error (\%)} \approx \frac{NG}{A_{VOL}} \bullet 100 \quad \text{Eq. 1-16}$$

Note that the expression of Eq. 1-16 is equivalent to the earlier mentioned Eq. 1-11, when  $1/\beta$  is substituted for NG. Again, either form can be used, at the user's discretion.

Notice from Eq. 1-16 that the percent gain error is directly proportional to the noise gain, therefore the effects of finite  $A_{VOL}$  are less for low gain. Some examples illustrate key points about these gain relationships.

In Figure 1-51, the first example for a NG of 1000 shows that for an open-loop gain of 2 million, the closed-loop gain error is about 0.05%. Note that if the open-loop gain stays constant over temperature and for various output loads and voltages, the 0.05% gain error can easily be calibrated out of the measurement, and then there is then no overall system gain error. If, however, the open-loop gain *changes*, the resulting closed-loop gain will also change. This introduces a *gain uncertainty*. In the second example,  $A_{VOL}$  drops to 300,000, which produces a gain error of 0.33%. This situation introduces a *gain uncertainty* of 0.28% in the closed-loop gain. In most applications, when using a good amplifier, the gain resistors of the circuit will be the largest source of absolute gain error, but it should be noted that gain uncertainty cannot be removed by calibration.

- “IDEAL” CLOSED LOOP GAIN =  $1/\beta$  = NOISE GAIN (NG)
- ACTUAL CLOSED LOOP GAIN =  $\frac{1}{\beta} \cdot \left| \frac{1}{1 + \frac{1}{A_{VOL}\beta}} \right| = \frac{NG}{1 + \frac{NG}{A_{VOL}}}$
- CLOSED LOOP GAIN ERROR (%)  $\approx \frac{NG}{A_{VOL}} \times 100 \quad (NG \ll A_{VOL})$ 
  - Ex. 1: Assume  $A_{VOL} = 2,000,000$ ,  $NG = 1,000$   
% Gain Error  $\approx 0.05\%$
  - Ex. 2: Assume  $A_{VOL}$  Drops to 300,000  
% Gain Error  $\approx 0.33\%$
  - Closed Loop Gain Uncertainty  
 $= 0.33\% - 0.05\% = 0.28\%$

**Figure 1-51: Changes in open-loop gain cause closed-loop gain uncertainty**

Changes in the output voltage level and output loading are the most common causes of changes in the open-loop gain of op amps. A change in open-loop gain with signal level produces a *nonlinearity* in the closed-loop gain transfer function, which also cannot be removed during system calibration. Most op amps have fixed loads, so  $A_{VOL}$  changes with load are not generally important. However, the sensitivity of  $A_{VOL}$  to output signal level may increase for higher load currents.

The severity of this nonlinearity varies widely from one device type to another, and generally isn't specified on the data sheet. The minimum  $A_{VOL}$  is always specified, and choosing an op amp with a high  $A_{VOL}$  will minimize the probability of gain nonlinearity errors. Gain nonlinearity can come from many sources, depending on the design of the op amp. One common source is thermal feedback (for example, from a hot output stage back to the input stage). If temperature shift is the sole cause of the nonlinearity error, it can be assumed that minimizing the output loading will help. To verify this, the nonlinearity is measured with no load, and then compared to the loaded condition.

An oscilloscope X-Y display test circuit for measuring dc open-loop gain nonlinearity is shown in Figure 1-52. The same precautions previously discussed relating to the offset voltage test circuit must also be observed in this circuit. The amplifier is configured for a signal gain of  $-1$ . The open-loop gain is defined as the change in output voltage divided by the change in the input offset voltage. However, for large values of  $A_{VOL}$ , the actual offset may change only a few microvolts over the entire output voltage swing. Therefore the divider consisting of the  $10\ \Omega$  resistor and  $R_G$  ( $1\ \text{M}\Omega$ ) forces the node voltage  $V_Y$  to be:

$$V_Y = \left[ 1 + \frac{R_G}{10\Omega} \right] V_{OS} = 100,001 \cdot V_{OS} \quad \text{Eq. 1-17}$$

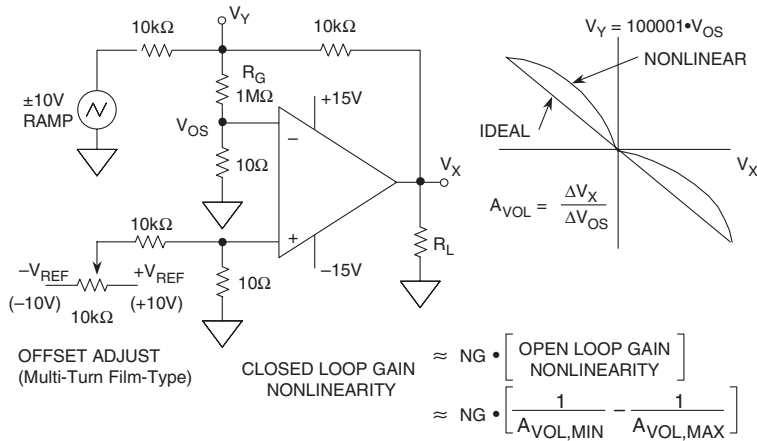


Figure 1-52: Circuit measures open-loop gain nonlinearity

The value of  $R_G$  is chosen to give measurable voltages at  $V_Y$ , depending on the expected values of  $V_{OS}$ .

The  $\pm 10$  V ramp generator output is multiplied by the signal gain,  $-1$ , and forces the op amp output voltage  $V_X$  to swing from  $+10$  V to  $-10$  V. Because of the gain factor applied to the offset voltage, the offset adjust potentiometer is added to allow the initial output offset to be set to zero. The resistor values chosen will null an input offset voltage of up to  $\pm 10$  mV. Stable 10 V voltage references such as the AD688 should be used at each end of the potentiometer to prevent output drift. *Note also that the ramp generator frequency must be quite low, probably no more than a fraction of 1 Hz because of the low corner frequency of the open-loop gain (0.1 Hz for the OP177).*

The plot on the right-hand side of Figure 1-52 shows  $V_Y$  plotted against  $V_X$ . If there is no gain nonlinearity, the graph will have a constant slope and  $A_{VOL}$  is calculated as follows:

$$A_{VOL} = \frac{\Delta V_X}{\Delta V_{OS}} = \left[ 1 + \frac{R_G}{10\Omega} \right] \left[ \frac{\Delta V_X}{\Delta V_Y} \right] = 100,001 \cdot \left[ \frac{\Delta V_X}{\Delta V_Y} \right]. \quad \text{Eq. 1-18}$$

If there is nonlinearity,  $A_{VOL}$  will vary dynamically as the output signal changes. The approximate open-loop gain nonlinearity is calculated based on the maximum and minimum values of  $A_{VOL}$  over the output voltage range:

$$\text{Open-Loop Gain Nonlinearity} = \frac{1}{A_{VOL,MIN}} - \frac{1}{A_{VOL,MAX}}. \quad \text{Eq. 1-19}$$

The closed-loop gain nonlinearity is obtained by multiplying the open-loop gain nonlinearity by the noise gain, NG:

$$\text{Closed-Loop Gain Nonlinearity} \approx NG \cdot \left[ \frac{1}{A_{VOL,MIN}} - \frac{1}{A_{VOL,MAX}} \right]. \quad \text{Eq. 1-20}$$

In an ideal case, the plot of  $V_{OS}$  versus  $V_X$  would have a constant slope, and the reciprocal of the slope is the open-loop gain,  $A_{VOL}$ . A horizontal line with zero slope would indicate infinite open-loop gain. In an actual op amp, the slope may change across the output range because of nonlinearity, thermal feedback, and so forth. In fact, the slope can even change sign.



Figure 1-53 shows the  $V_Y$  (and  $V_{OS}$ ) versus  $V_X$  plot for an OP177 precision op amp. The plot is shown for two different loads, 2 k $\Omega$  and 10 k $\Omega$ . The reciprocal of the slope is calculated based on the end points, and the average  $A_{VOL}$  is about 8 million. The maximum and minimum values of  $A_{VOL}$  across the output voltage range are measured to be approximately 9.1 million, and 5.7 million, respectively. This corresponds to an open-loop gain nonlinearity of about 0.07 ppm. Thus, for a noise gain of 100, the corresponding closed-loop gain nonlinearity is about 7 ppm.

These nonlinearity measurements are, of course, most applicable to high precision dc circuits. But they are also applicable to wider bandwidth applications, such as audio. The X-Y display technique of Figure 1-52 will easily show for example, crossover distortion in a poorly designed op amp output stage.

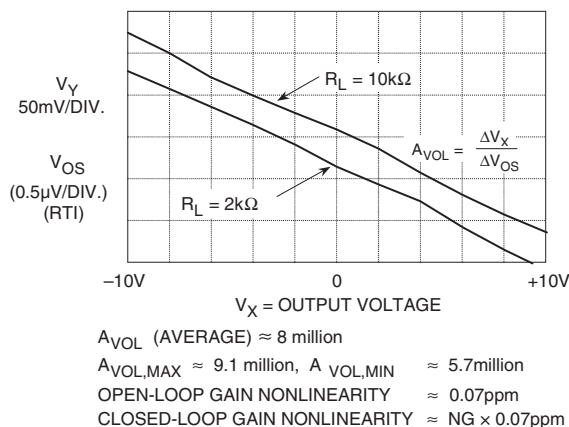


Figure 1-53: OP177 gain nonlinearity

## Op Amp Frequency Response

There are a number of issues to consider when discussing the frequency response of op amps. Some are relevant to both voltage and current feedback op amp types, some apply to one or the other, but not to both. Issues that vary with type are usually related to small signal performance, while large-signal issues mostly apply to both.

A good working definition of “large-signal” is where the output voltage swing/frequency limit is set by the slew rate measured at the output stage, rather than the pole(s) of the small signal response. We shall therefore consider large signal parameters applying to both types of op amp before we consider those parameters where they differ.

### Frequency Response—Slew Rate and Full-Power Bandwidth

The slew rate (SR) of an amplifier is the maximum rate of change of voltage at its output. It is expressed in V/s (or, more probably, V/ $\mu$ s). We have mentioned earlier why op amps might have different slew rates during positive-and negative-going transitions, but for this analysis we shall assume that good fast op amps have reasonably symmetrical slew rates.

If we consider a sine wave signal with a peak-to-peak amplitude of  $2 V_p$  and of a frequency  $f$ , the expression for the output voltage is:

$$V(t) = V_p \sin 2\pi ft. \quad \text{Eq. 1-21}$$

This sine wave signal has a maximum rate of change (slope) at the zero crossing. This maximum rate of change is:

$$\left. \frac{dV}{dt} \right|_{\max} = 2\pi f V_p \quad \text{Eq. 1-22}$$

To reproduce this signal without distortion, an amplifier must be able to respond in terms of its output voltage at this rate (or faster). When an amplifier reaches its maximum output rate of change, or *slew rate*, it is said to be *slew limiting* (sometimes also called rate limiting). Thus, we can see that the maximum signal frequency at which slew limiting *does not* occur is directly proportional to the signal slope, and inversely proportional to the amplitude of the signal. This allows us to define the *full power bandwidth* (FPBW) of an op amp, which is the maximum frequency at which slew limiting doesn't occur for rated voltage output. It is calculated by letting  $2 V_p$  in Eq. 1-22 equal the maximum peak-to-peak swing of the amplifier,  $dV/dt$  equal the amplifier slew rate, and solving for  $f$ :

$$\text{FPBW} = \text{Slew Rate} / 2\pi V_p \quad \text{Eq. 1-23}$$

It is important to realize that both slew rate and full-power bandwidth can also depend somewhat on the power supply voltage being used, and the load the amplifier is driving (particularly if it is capacitive).

The key issues regarding slew rate and full-power bandwidth are summarized in Figure 1-54. As a point of reference, an op amp with a 1 V peak output swing reproducing a 1MHz sine wave must have a minimum SR of 6.28 V/ $\mu$ s.

- Slew Rate = Maximum rate at which the output voltage of an op amp can change
- Ranges: A few volts/ $\mu$ s to several thousand volts/ $\mu$ s
- For a sinewave,  $V_{\text{OUT}} = V_p \sin 2\pi ft$ 

$$dV/dt = 2\pi f V_p \cos 2\pi ft$$

$$(dV/dt)_{\max} = 2\pi f V_p$$
- If  $2V_p$  = full output span of op amp, then
 
$$\text{Slew Rate} = (dV/dt)_{\max} = 2\pi \cdot \text{FPBW} \cdot V_p$$

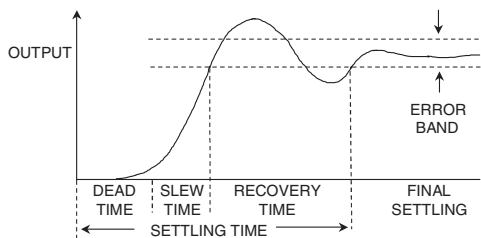
$$\text{FPBW} = \text{Slew Rate} / 2\pi V_p$$

**Figure 1-54: Slew rate and full-power bandwidth**

Realistically, for a practical circuit the designer would choose an op amp with an SR in excess of this figure, since real op amps show increasing distortion prior to reaching the slew limit point.

## Frequency Response—Settling Time

The *settling time* of an amplifier is defined as the time it takes the output to respond to a step change of input and *come into, and remain within, a defined error band*, as measured relative to the 50% point of the input pulse, as shown in Figure 1-55.



- Error band is usually defined to be a percentage of the step 0.1%, 0.05%, 0.01%, etc.
- Settling time is nonlinear; it may take 30 times as long to settle to 0.01% as to 0.1%.
- Manufacturers often choose an error band that makes the op amp look good.

**Figure 1-55: Settling time**

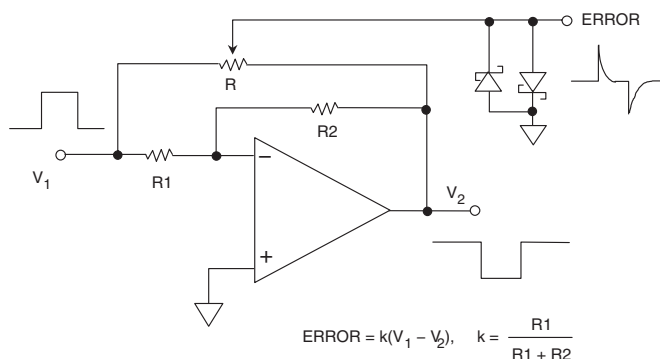
Unlike a DAC device, there is no natural error band for an op amp (a DAC naturally has an error band of 1 LSB, or perhaps  $\pm 1$  LSB). So, one must be chosen and defined, along with other definitions, such as the step size (1 V, 5 V, 10 V, and so forth). What is chosen will depend on the performance of the op amp, but since the value chosen will vary from device to device, comparisons are often difficult. This is true because settling is not linear, and many different time constants may be involved. Examples are early op amps using dielectrically isolated (DI) processes. These had very fast settling to 1% of full scale, but they took almost forever to settle to 10 bits (0.1 %). Similarly, some very high precision op amps have thermal effects that cause settling to 0.001% or better to take tens of ms, although they will settle to 0.025% in a few  $\mu$ s.

It should also be noted that thermal effects can cause significant differences between short-term settling time (generally measured in nanoseconds) and long-term settling time (generally measured in microseconds or milliseconds). In many ac applications, long-term settling time is not important; but if it is, it must be measured on a much different time scale than short-term settling time.

Measuring fast settling time to high accuracy is very difficult. Great care is required in order to generate fast, highly accurate, low noise, flat-top pulses. Large amplitude step voltages will overdrive many oscilloscope front ends, when the input scaling is set for high sensitivity.

The example test setup shown in Figure 1-56 is useful in making settling time measurements on op amps operating in the inverting mode. The signal at the “false summing node” represents the difference between the output and the input signal, multiplied by the constant  $k$ , i.e., the ERROR signal.

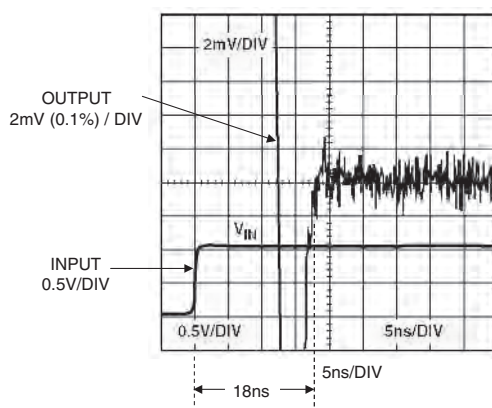
Many subtleties are involved in making this setup work reliably. The resistances should low in value, to minimize parasitic time constants. The back-back Schottky diode clamps help prevent scope overdrive, and allow high sensitivity. If  $R1 = R2$ , then  $k = 0.5$ . Thus the error band at the ERROR output will be 5 mV for 0.1% settling with a 10 V input step.



**Figure 1-56: Measuring settling time using a “false summing node”**

In some cases, a second (very fast) amplifier stage may be used after the false summing node, to increase the signal level. In any case, to ensure validity, testing of settling time must be done with a test setup identical to that used by the op amp manufacturer.

Many modern digitizing oscilloscopes are insensitive to input overdrive and can be used to measure the ERROR waveform directly—this must be verified for each oscilloscope by carefully examining the operating manual. Note that a direct measurement allows measurements of settling time in both the inverting and noninverting modes. An example of the output step response to a flat pulse input for the AD8039 op amp is shown in Figure 1-57. Notice that the settling time to 0.1% is approximately 18 ns.



**Figure 1-57: AD8039  $G = +2$  settling time measured directly**

In making settling time measurements of this type, it is also imperative to use a pulse generator source capable of generating a pulse of sufficient flatness. In other words, if the op amp under test has a settling time of 20 ns to 0.1%, the applied pulse should settle to better than 0.05% in less than 5 ns.

This type of generator can be expensive, but a simple circuit, as shown in Figure 1-58, can be used with a reasonably flat generator to ensure a flat pulse output.

The circuit of Figure 1-58 works best if low capacitance Schottky diodes are used for D1–D2–D3, and the lead lengths on all the connections are minimized. A short length of 50  $\Omega$  coax can be used to connect the pulse generator to the circuit; however, best results are obtained if the test fixture is connected directly to the output of the generator. The pulse generator is adjusted to output a positive-going pulse at “A” which rises from approximately  $-1.8$  V to  $+0.5$  V in less than 5 ns (assuming the settling time of the DUT is in the order of 20 ns). Shorter rise times may generate ringing, and longer rise times can degrade the DUT settling time; therefore, some optimization is required in the actual circuit to get best performance. When the pulse generator output “A” goes above 0 V, D1 begins to conduct, and D2/D3 are reverse biased. The “0 V” region of the signal “B” at the input of the DUT is flat “by definition”—neglecting the leakage current and stray capacitance of the D2–D3 series combination. The D1 diode and its 100  $\Omega$  resistor help maintain an approximate 50  $\Omega$  termination during the time the pulse at “A” is positive.

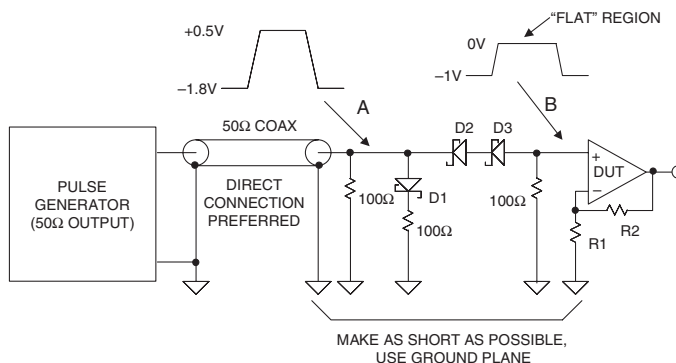


Figure 1-58: A simple flat pulse generator

## Frequency Response—Voltage Feedback Op amps, Gain-Bandwidth Product

The open-loop frequency response of a voltage feedback op amp is shown in Figure 1-59. There are two possibilities: Figure 1-59A shows the most common, where a high dc gain drops at 6 dB/octave from quite a low frequency down to unity gain. This is a classic single pole response. By contrast, the amplifier in Figure 1-59B has two poles in its response—gain drops at 6 dB/octave for a while, and then drops at

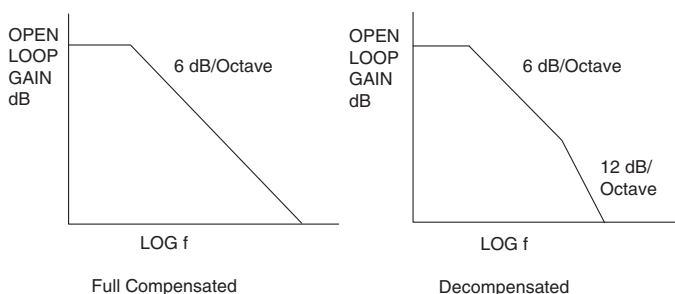


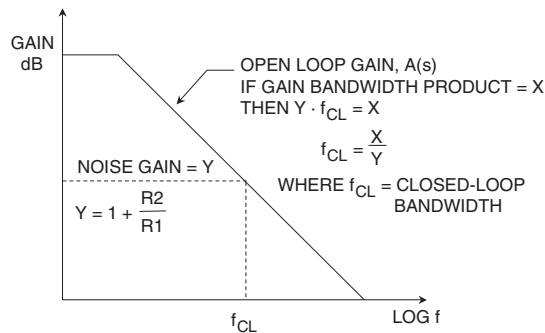
Figure 1-59: Frequency response of voltage feedback op amps

12 dB/octave. The amplifier in Figure 1-59A is known as an *unconditionally stable* or *fully compensated* type and may be used with a noise gain of unity. This type of amplifier is stable with 100% feedback (including capacitance) from output to inverting input.

Compare this to the amplifier in Figure 1-59B. If this op amp is used with a noise gain that is lower than the gain at which the slope of the response increases from 6 dB to 12 dB/octave, the phase shift in the feedback will be too great, and it will oscillate. Amplifiers of this type are characterized as “stable at gains  $\geq X$ ” where  $X$  is the gain at the frequency where the 6 dB/12 dB transition occurs. Note that here it is, of course, the *noise gain* that is being referenced. The gain level for stability might be between 2 and 25, typically quoted behavior might be “gain-of-five-stable,” and so forth. These *decompensated* op amps do have higher gain bandwidth products than fully compensated amplifiers, all other things being equal. So they are useful, despite the slightly greater complication of designing with them. But, unlike their fully compensated op amp relatives, a decompensated op amp can never be used with direct capacitive feedback from output to inverting input.

The 6 dB/octave slope of the response of both types means that over the range of frequencies where this slope occurs, *the product of the closed-loop gain and the 3 dB closed-loop bandwidth at that gain is a constant*—this is known as the *gain bandwidth product* (GBW) and is a figure of merit for an amplifier.

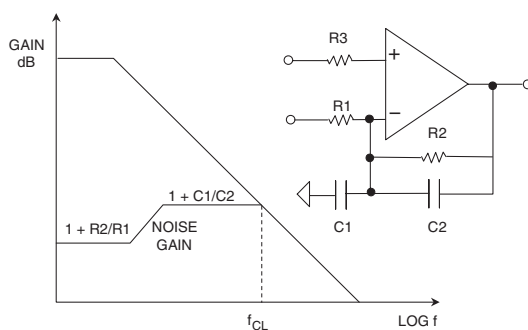
For example, if an op amp has a GBW product of  $X$  MHz, its closed-loop bandwidth at a noise gain of 1 will be  $X$  MHz, at a noise gain of 2 it will be  $X/2$  MHz, and at a noise gain of  $Y$  it will be  $X/Y$  MHz (see Figure 1-60). Notice that the *closed-loop* bandwidth is the frequency at which the noise gain plateau intersects the open-loop gain.



**Figure 1-60: Gain-bandwidth product for voltage feedback op amps**

In the above example, it was assumed that the feedback elements were resistive. This is not usually the case, especially when the op amp requires a feedback capacitor for stability.

Figure 1-61 shows a typical example where there is capacitance,  $C1$ , on the inverting input of the op amp. This capacitance is the sum of the op amp internal capacitance, plus any external capacitance that may exist. This always-present capacitance introduces a pole in the noise gain transfer function.



**Figure 1-61: Bode plot showing noise gain for voltage feedback op amp with resistive and reactive feedback elements**

The net slope of the noise gain curve and the open-loop gain curve, *at the point of intersection*, determines system stability. For unconditional stability, the noise gain must intersect the open-loop gain with a net slope of less than 12 dB/octave (20 dB per decade). Adding the feedback capacitor,  $C2$ , introduces a zero in the noise gain transfer function, which stabilizes the circuit. Notice that in Figure 1-61 the closed-loop bandwidth,  $f_{cl}$ , is the frequency at which the noise gain intersects the open-loop gain.

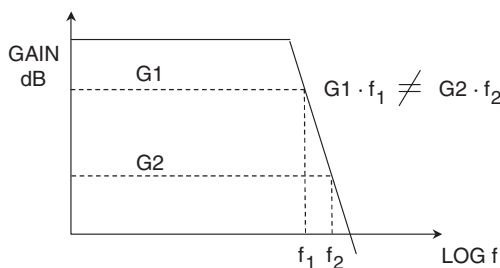
The Bode plot of the noise gain is a very useful tool in analyzing op amp stability. Constructing the Bode plot is a relatively simple matter. Although it is outside the scope of this section to carry the discussion of noise gain and stability further, the reader is referred to Reference 1 for an excellent treatment of constructing and analyzing Bode plots. Second-order systems related to noise analysis are discussed later in this section.

## Frequency Response—Current Feedback Op Amps

Current feedback op amps do not behave in the same way as voltage feedback types. They are not stable with capacitive feedback, nor are they so with a short circuit from output to inverting input. With a CFB op amp, *there is generally an optimum feedback resistance for maximum bandwidth*. Note that the value of this resistance may vary with supply voltage—consult the device data sheet. If the feedback resistance is increased, the bandwidth is reduced. Conversely, if it is reduced, bandwidth increases, and the amplifier may become unstable.

In a CFB op amp, for a given value of feedback resistance ( $R2$ ), *the closed-loop bandwidth is largely unaffected by the noise gain*, as shown in Figure 1-62. Thus it is not correct to refer to gain bandwidth product, for a CFB amplifier, because of the fact that it is not constant. Gain is manipulated in a CFB op amp application by choosing the correct feedback resistor for the device ( $R2$ ), and then selecting the bottom resistor ( $R1$ ) to yield the desired closed loop gain. The gain relationship of  $R2$  and  $R1$  is identical to the case of a VFB op amp (Figure 1-14).

Typically, CFB op amp data sheets will provide a table of recommended resistor values that provide maximum bandwidth for the device, over a range of both gain and supply voltage. It simplifies the design process considerably to use these tables.



- Feedback resistor fixed for optimum performance. Larger values reduce bandwidth, smaller values may cause instability.
- For fixed feedback resistor, changing gain has little effect on bandwidth.
- Current feedback op amps do not have a fixed gain-bandwidth product.

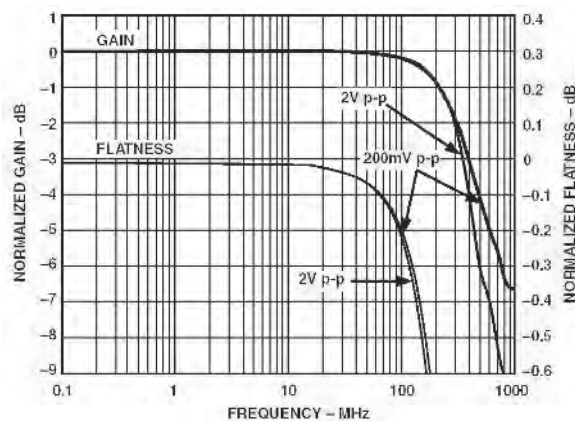
Figure 1-62: Frequency response for current feedback op amps

## Bandwidth Flatness

In demanding applications such as professional video, it is desirable to maintain a relatively flat bandwidth and linear phase up to some maximum specified frequency, and simply specifying the 3dB bandwidth isn't enough. In particular, it is customary to specify the *0.1 dB bandwidth*, or *0.1 dB bandwidth flatness*. This means there is no more than 0.1 dB ripple up to a specified 0.1 dB bandwidth frequency.

Video buffer amplifiers generally have both the 3 dB and the 0.1 dB bandwidth specified. Figure 1-63 shows the frequency response of the AD8075 triple video buffer.

Note that the 3 dB bandwidth is approximately 400 MHz. This can be determined from the response labeled "GAIN" in the graph, and the corresponding gain scale is shown on the left-hand vertical axis (at a scaling of 1 dB/division).



3dB BANDWIDTH  $\approx$  400MHz, 0.1dB BANDWIDTH  $\approx$  65MHz

Figure 1-63: 3 dB and 0.1 dB bandwidth for the AD8075,  $G = 2$ , triple video buffer,  $R_L = 150 \Omega$



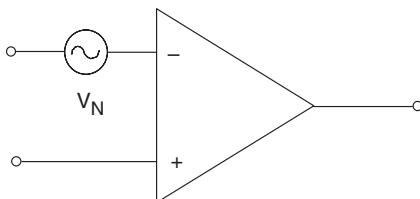
The response scale for “FLATNESS” is on the right-hand vertical axis, at a scaling of 0.1 dB/division in this case. This allows the 0.1 dB bandwidth to be determined, which is about 65 MHz in this case. The general point to be noted here is the major difference in the applicable bandwidth between the 3 dB and 0.1 dB criteria. It requires a 400 MHz bandwidth amplifier (as conventionally measured) to provide the 65 MHz 0.1 dB flatness rating.

It should be noted that these specifications hold true when driving a  $75\ \Omega$  source and load terminated cable, which represents a resistive load of  $150\ \Omega$ . Any capacitive loading at the amplifier output will cause peaking in the frequency response, and must be avoided.

## Operational Amplifier Noise

This section discusses the noise generated within op amps, not the external noise they may pick up. External noise is also important, and is discussed in detail in Chapter 7; in this section we are concerned solely with internal noise.

There are three noise sources in an op amp: a voltage noise, which appears differentially across the two inputs, and two current noise sources, one in each input. The simple voltage noise op amp model is shown in Figure 1-64. The three noise sources are effectively uncorrelated (independent of each other). There is a slight correlation between the two noise currents, but it is too small to need consideration in practical noise analyses. In addition to these three internal noise sources, it is necessary to consider the Johnson noise of the external gain-setting resistors that are used with the op amp.



- Input Voltage Noise is bandwidth dependent and measured in  $\text{nV}/\sqrt{\text{Hz}}$  (noise spectral density)
- Normal Ranges are  $1\ \text{nV}/\sqrt{\text{Hz}}$  to  $20\ \text{nV}/\sqrt{\text{Hz}}$

**Figure 1-64: Input voltage noise**

All resistors have a Johnson noise of  $\sqrt{4kTB R}$  where  $k$  is Boltzmann’s Constant ( $1.38 \times 10^{-23}\text{J/K}$ ),  $T$  is the absolute temperature,  $B$  is the bandwidth, and  $R$  is the resistance. Note that this is an intrinsic property—it is not possible to obtain resistors that do not have Johnson noise. The simple model is shown in Figure 1-65.

Uncorrelated noise voltages add in a “root-sum-of-squares” manner; i.e., noise voltages  $V_1$ ,  $V_2$ ,  $V_3$  give a summed result of  $\sqrt{V_1^2 + V_2^2 + V_3^2}$ . Noise powers, of course, add normally. Thus, any noise voltage that is more than 3 to 5 times any of the others is dominant, and the others may generally be ignored. This simplifies noise assessment. The voltage noise of different op amps may vary from under  $1\ \text{nV}/\sqrt{\text{Hz}}$  to  $20\ \text{nV}/\sqrt{\text{Hz}}$ , or even more. Bipolar op amps tend to have lower voltage noise than JFETs, although it is possible to make JFET op amps with low voltage noise (such as the AD743/AD745), at the cost of large input devices, and hence large input capacitance. Voltage noise is specified on the data sheet, and it isn’t possible to predict it from other parameters.

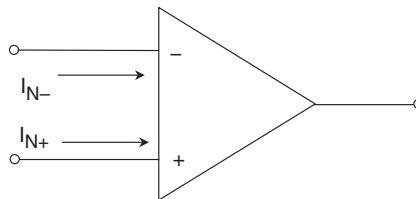


- ALL resistors have a voltage noise of  $V_{NR} = \sqrt{4kTB R}$
- $T$  = Absolute Temperature =  $T(^{\circ}\text{C}) + 273.15$
- $B$  = Bandwidth (Hz)
- $k$  = Boltzmann's Constant ( $1.38 \times 10^{-23} \text{ J/K}$ )
- A  $1000 \, \Omega$  resistor generates  $4 \text{ nV}/\sqrt{\text{Hz}}$  @  $25^{\circ}\text{C}$

**Figure 1-65: Johnson noise of resistors**

Current noise can vary much more widely, dependent upon the input structure. It ranges from around  $0.1 \text{ fA}/\sqrt{\text{Hz}}$  (in JFET electrometer op amps) to several  $\text{pA}/\sqrt{\text{Hz}}$  (in high speed bipolar op amps). It isn't always specified on data sheets, but may be calculated in cases like simple BJT or JFETs, where all the bias current flows in the input junction, because in these cases it is simply the Schottky (or shot) noise of the bias current.

Shot noise spectral density is simply  $\sqrt{(2I_b q)}/\sqrt{\text{Hz}}$ , where  $I_b$  is the bias current (in amps) and  $q$  is the charge on an electron ( $1.6 \times 10^{-19} \text{ C}$ ). It can't be calculated for bias-compensated or current feedback op amps, where the external bias current is the *difference* of two internal currents. A simple current noise model is shown in Figure 1-66.



- Normal Ranges:  $0.1 \text{ fA}/\sqrt{\text{Hz}}$  to  $10 \text{ pA}/\sqrt{\text{Hz}}$
- In Voltage Feedback op amps, the current noise in the inverting and noninverting inputs is uncorrelated (effectively) but roughly equal in magnitude.
- In simple BJT and JFET input stages, the current noise is the shot noise of the bias current and may be calculated from the bias current.
- In bias-compensated input stages and in current feedback op amps, the current noise cannot be calculated.
- The current noise in the two inputs of a current feedback op amp may be quite different. They may not even have the same  $1/f$  corner.

**Figure 1-66: Input current noise**

Current noise is only important when it flows in an impedance, and thus generates a noise voltage. Maintaining relatively low impedances at the input of an op amp circuit contributes markedly to minimizing the effects of current noise (just as doing the same thing also aids in minimizing offset voltage).

It is logical therefore that the optimum choice of a low noise op amp depends on the impedances around it. This will be illustrated with the aid of some impedance examples, immediately below.

Consider for example an OP27, an op amp with low voltage noise ( $3\text{ nV}/\sqrt{\text{Hz}}$ ), but quite high current noise ( $1\text{ pA}/\sqrt{\text{Hz}}$ ). With zero source impedance, the voltage noise will dominate as shown in Figure 1-67 (left column). With a source resistance of  $3\text{ k}\Omega$  (center column), the current noise of ( $1\text{ pA}/\sqrt{\text{Hz}}$ ) flowing in  $3\text{ k}\Omega$  will equal the voltage noise, but the Johnson noise of the  $3\text{ k}\Omega$  resistor is ( $7\text{ nV}/\sqrt{\text{Hz}}$ ) and is dominant. With a source resistance of  $300\text{ k}\Omega$  (right column), the current noise portion increases  $100\times$  to  $300\text{ nV}/\sqrt{\text{Hz}}$ , voltage noise continues unchanged, and the Johnson noise (which is proportional to the resistance *square root*) increases tenfold. Current noise dominates.

The above example shows that the choice of a low noise op amp depends on the source impedance of the signal, and at high impedances, current noise always dominates.

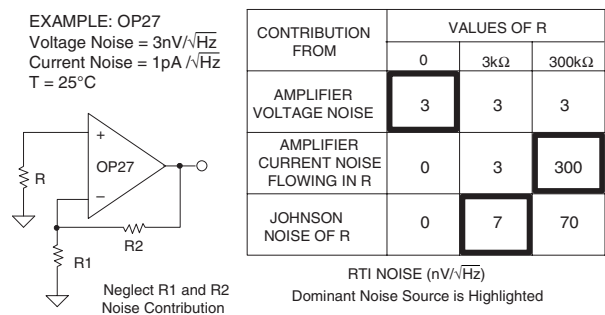
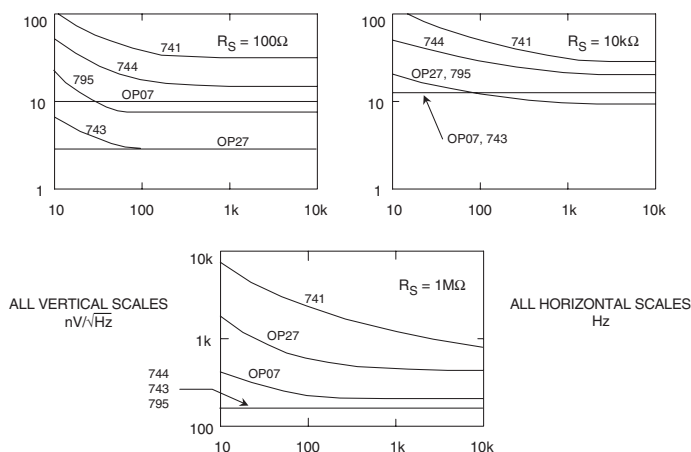


Figure 1-67: Different noise sources dominate at different source impedances

From Figure 1-68, it should be apparent that different amplifiers are best at different source impedances. For low impedance circuits, low voltage noise amplifiers such as the OP27 will be the obvious choice, since they are inexpensive, and their comparatively large current noise will not affect the application. At medium resistances, the Johnson noise of resistors is dominant, while at very high source resistance, we must choose an op amp with the smallest possible current noise, such as the AD549 or AD795.

Until recently, BiFET amplifiers tended to have comparatively high voltage noise (though very low current noise), and were thus more suitable for low noise applications in high rather than low impedance circuitry. The AD795, AD743, and AD745 have very low values of both voltage and current noise. The AD795 specifications at  $10\text{ kHz}$  are  $10\text{ nV}/\sqrt{\text{Hz}}$  and  $0.6\text{ fA}/\sqrt{\text{Hz}}$ , and the AD743/AD745 specifications at  $10\text{ kHz}$  are  $2.9\text{ nV}/\sqrt{\text{Hz}}$  and  $6.9\text{ fA}/\sqrt{\text{Hz}}$ . These make possible the design of low-noise amplifier circuits that have low noise over a wide range of source impedances.

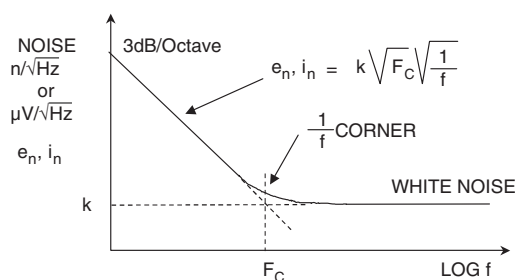
The *noise figure* of an amplifier is the amount (in dB) by which the noise of the amplifier exceeds the noise of a perfect noise-free amplifier in the same environment. The concept is useful in RF and TV applications, where  $50\text{ }\Omega$  and  $75\text{ }\Omega$  transmission lines and terminations are ubiquitous, but is useless for an op amp that is used in a wide range of electronic environments. Noise figure related to communications applications is discussed in more detail in Chapter 6 (Section 6-4). Voltage noise spectral density and current noise spectral density are generally more useful specifications in most cases.



**Figure 1-68: Different amplifiers are best at different source impedances**

So far, we have assumed that noise is *white* (i.e., its spectral density does not vary with frequency). This is true over most of an op amp's frequency range, but at low frequencies the noise spectral density rises at 3 dB/octave, as shown in Figure 1-69. The power spectral density in this region is inversely proportional to frequency, and therefore the voltage noise spectral density is inversely proportional to the square root of the frequency. For this reason, this noise is commonly referred to as *1/f noise*. Note, however, that some textbooks still use the older term *flicker noise*.

The frequency at which this noise starts to rise is known as the *1/f corner frequency* ( $F_C$ ) and is a figure of merit—the lower it is, the better. The *1/f* corner frequencies are not necessarily the same for the voltage noise and the current noise of a particular amplifier, and a current feedback op amp may have three *1/f* corners: for its voltage noise, its inverting input current noise, and its noninverting input current noise.



- *1/f* Corner Frequency is a figure of merit for op amp noise performance (the lower the better)
- Typical Ranges: 2Hz to 2kHz
- Voltage Noise and Current Noise do not necessarily have the same *1/f* corner frequency

**Figure 1-69: Frequency characteristic of op amp noise**

The general equation which describes the voltage or current noise spectral density in the 1/f region is

$$e_n, i_n = k\sqrt{F_c} \sqrt{\frac{1}{f}}, \quad \text{Eq. 1-24}$$

where  $k$  is the level of the “white” current or voltage noise level, and  $F_c$  is the 1/f corner frequency.

The best low frequency low noise amplifiers have corner frequencies in the range 1 Hz–10 Hz, while JFET devices and more general-purpose op amps have values in the range to 100 Hz. Very fast amplifiers however may make compromises in processing to achieve high speed which result in quite poor 1/f corners of several hundred Hz or even 1 kHz–2 kHz. This is generally unimportant in the wideband applications for which they were intended, but may affect their use at audio frequencies, particularly for equalized circuits.

## Popcorn Noise

*Popcorn noise* is so-called because when played through an audio system, it sounds like cooking popcorn. It consists of random step changes of offset voltage that take place at random intervals in the 10+ millisecond timeframe. Such noise results from high levels of contamination and crystal lattice dislocation at the surface of the silicon chip, which in turn results from inappropriate processing techniques or poor quality raw materials.

When monolithic op amps were first introduced in the 1960s, popcorn noise was a dominant noise source. Today, however, the causes of popcorn noise are well understood, raw material purity is high, contamination is low, and production tests for it are reliable so that no op amp manufacturer should have any difficulty in shipping products that are substantially free of popcorn noise. For this reason, it is not even mentioned in most modern op amp textbooks.

## RMS Noise Considerations

As was discussed above, noise spectral density is a function of frequency. In order to obtain the RMS noise, the noise spectral density curve must be integrated over the bandwidth of interest.

In the 1/f region, the RMS noise in the bandwidth  $F_L$  to  $F_c$  is given by

$$v_{n,rms}(F_L, F_c) = v_{nw} \sqrt{F_c} \sqrt{\int_{F_L}^{F_c} \frac{1}{f} df} = v_{nw} \sqrt{F_c \ln \left[ \frac{F_c}{F_L} \right]} \quad \text{Eq. 1-25}$$

where  $v_{nw}$  is the voltage noise spectral density in the “white” region,  $F_L$  is the lowest frequency of interest in the 1/f region, and  $F_c$  is the 1/f corner frequency.

The next region of interest is the “white” noise area which extends from  $F_c$  to  $F_H$ .

The RMS noise in this bandwidth is given by

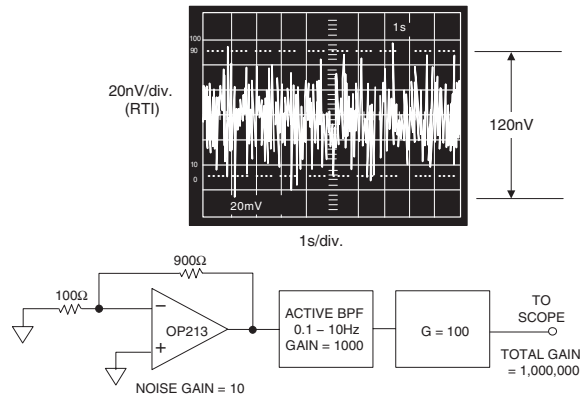
$$v_{n,rms}(F_c, F_H) = v_{nw} \sqrt{F_H - F_c} \quad \text{Eq. 1-26}$$

Eq. 1-25 and Eq. 1-26 can be combined to yield the total RMS noise from  $F_L$  to  $F_H$ :

$$v_{n,rms}(F_L, F_H) = v_{nw} \sqrt{F_c \ln \left[ \frac{F_c}{F_L} \right] + (F_H - F_c)} \quad \text{Eq. 1-27}$$

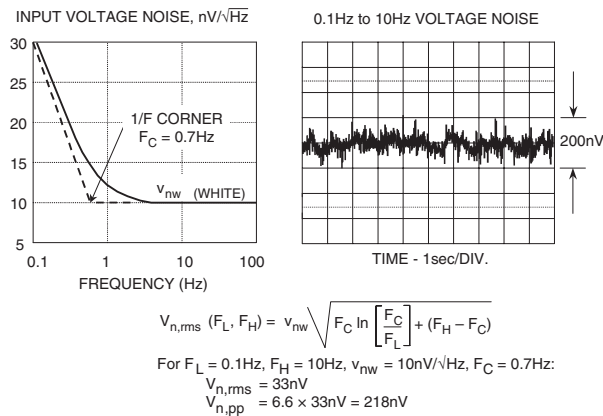
In many cases, the low frequency p-p noise is specified in a 0.1 Hz to 10 Hz bandwidth, measured with a 0.1 Hz to 10 Hz bandpass filter between op amp and measuring device.

The measurement is often presented as a scope photo with a time scale of 1s/div, as shown in Figure 1-70 for the OP213.



**Figure 1-70: The peak-to-peak noise in the 0.1 Hz to 10 Hz bandwidth for the OP213 is less than 120 nV**

It is possible to relate the  $1/f$  noise measured in the 0.1 Hz to 10 Hz bandwidth to the voltage noise spectral density. Figure 1-71 shows the OP177 input voltage noise spectral density on the left-hand side of the diagram, and the 0.1 Hz to 10 Hz peak-to-peak noise scope photo on the right-hand side. Eq. 1-26 can be used to calculate the total RMS noise in the bandwidth 0.1 Hz to 10 Hz by letting  $F_L = 0.1$  Hz,  $F_H = 10$  Hz,  $F_C = 0.7$  Hz,  $v_{nw} = 10 \text{ nV}/\sqrt{\text{Hz}}$ . The value works out to be about 33 nV RMS, or 218 nV peak-to-peak (obtained by multiplying the RMS value by 6.6—see the following discussion). This compares well to the value of 200 nV as measured from the scope photo.



**Figure 1-71: Input voltage noise for the OP177**

It should be noted that at higher frequencies, the term in the equation containing the natural logarithm becomes insignificant, and the expression for the RMS noise becomes:

$$V_{n,rms}(F_H, F_L) \approx v_{nw} \sqrt{F_H - F_L} \quad \text{Eq. 1-28}$$

And, if  $F_H \gg F_L$ ,

$$V_{n,rms}(F_H) \approx v_{nw} \sqrt{F_H} \quad \text{Eq. 1-29}$$

However, some op amps (such as the OP07 and OP27) have voltage noise characteristics that increase slightly at high frequencies. The voltage noise versus frequency curve for op amps should therefore be examined carefully for flatness when calculating high frequency noise using this approximation.

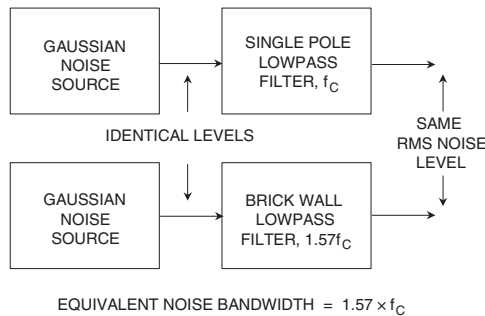
At very low frequencies when operating exclusively in the  $1/f$  region,  $F_C \gg (F_H - F_L)$ , and the expression for the RMS noise reduces to:

$$V_{n,rms}(F_H, F_L) \approx V_{nw} \sqrt{F_C \ln \left[ \frac{F_H}{F_L} \right]}. \quad \text{Eq. 1-30}$$

Note that there is no way of reducing this  $1/f$  noise by filtering if operation extends to dc. Making  $F_H = 0.1$  Hz and  $F_L = 0.001$  still yields an RMS  $1/f$  noise of about 18 nV RMS, or 119 nV peak-to-peak.

The point is that averaging results of a large number of measurements over a long period of time has practically no effect on the RMS value of the  $1/f$  noise. A method of reducing it further is to use a chopper-stabilized op amp, to remove the low frequency noise.

In practice, it is virtually impossible to measure noise within specific frequency limits with no contribution from outside those limits, since practical filters have finite roll-off characteristics. Fortunately, measurement error introduced by a single pole low-pass filter is readily computed. The noise in the spectrum above the single pole filter cutoff frequency,  $f_c$ , extends the corner frequency to  $1.57 f_c$ . Similarly, a two pole filter has an apparent corner frequency of approximately  $1.2 f_c$ . The error correction factor is usually negligible for filters having more than two poles. The net bandwidth after the correction is referred to as the filter *equivalent noise bandwidth* (see Figure 1-72).



**Figure 1-72: Equivalent noise bandwidth**

It is often desirable to convert RMS noise measurements into peak-to-peak. In order to do this, one must have some understanding of the statistical nature of noise. For Gaussian noise and a given value of RMS noise, statistics tell us that the chance of a particular peak-to-peak value being exceeded decreases sharply as that value increases—but this probability never becomes zero.

Thus, for a given RMS noise, it is possible to predict the percentage of time that a given peak-to-peak value will be exceeded, but it is not possible to give a peak-to-peak value which will never be exceeded as shown in Figure 1-73.

Nominal Peak-to-Peak	% of the Time Noise will Exceed Nominal Peak-to-Peak Value
$2 \times \text{rms}$	32%
$3 \times \text{rms}$	13%
$4 \times \text{rms}$	4.6%
$5 \times \text{rms}$	1.2%
$6 \times \text{rms}$	0.27%
$6.6 \times \text{rms}^*$	0.10%
$7 \times \text{rms}$	0.046%
$8 \times \text{rms}$	0.006%

\*Most often used conversion factor is 6.6

**Figure 1-73: RMS to peak-to-peak ratios**

Peak-to-peak noise specifications, therefore, must always be written with a time limit. A suitable one is 6.6 times the RMS value, which is exceeded only 0.1% of the time.

### Total Output Noise Calculations

We have already pointed out that any noise source that produces less than one-third to one-fifth of the noise of some greater source can be ignored, with little error. When so doing, both noise voltages must be measured at the same point in the circuit. To analyze the noise performance of an op amp circuit, we must assess the noise contributions of each part of the circuit, and determine which are significant. To simplify the following calculations, we shall work with noise spectral densities, rather than actual voltages, to leave bandwidth out of the expressions (the noise spectral density, which is generally expressed in  $\mu\text{V}/\sqrt{\text{Hz}}$ , is equivalent to the noise in a 1 Hz bandwidth).



If we consider the circuit in Figure 1-74, which is an amplifier consisting of an op amp and three resistors (R3 represents the source resistance at node A), we can find six separate noise sources: the Johnson noise of the three resistors, the op amp voltage noise, and the current noise in each input of the op amp. Each source has its own contribution to the noise at the amplifier output. Noise is generally specified RTI, or *referred to the input*, but it is often simpler to calculate the noise referred to the output (RTO) and then divide it by the *noise* gain (not the *signal* gain) of the amplifier to obtain the RTI noise.

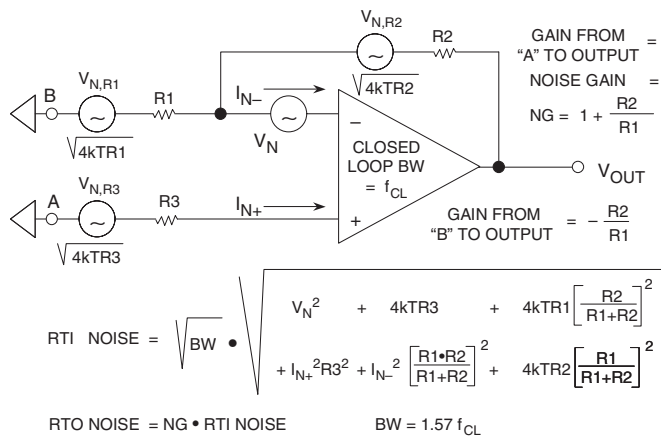


Figure 1-74: Op amp noise model for single-pole system

Figure 1-75 is a detailed analysis of how each of the noise sources in Figure 1-74 is reflected to the output of the op amp. Some further discussion regarding the effect of the current noise at the inverting input is warranted. This current,  $I_{N-}$ , does not flow in R1, as might be expected—the negative feedback around the amplifier works to keep the potential at the inverting input unchanged, so that a current flowing from that pin is forced, by negative feedback, to flow in R2 only, resulting in a voltage at the output of  $I_{N-} R_2$ . We could equally well consider the voltage caused by  $I_{N-}$  flowing in the parallel combination of R1 and R2 and then amplified by the noise gain of the amplifier, but the results are identical—only the calculations are more involved.

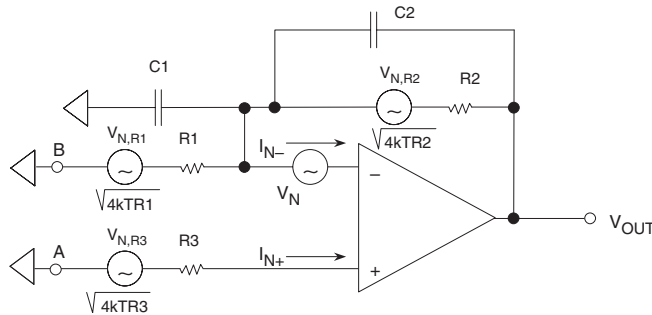
NOISE SOURCE EXPRESSED AS A VOLTAGE	MULTIPLY BY THIS FACTOR TO REFER TO THE OP AMP OUTPUT
Johnson noise in R3: $\sqrt{(4kTR_3)}$	Noise Gain = $1 + R_2/R_1$
Noninverting input current noise flowing in R3: $I_{N+} R_3$	Noise Gain = $1 + R_2/R_1$
Input voltage noise: $V_N$	Noise Gain = $1 + R_2/R_1$
Johnson noise in R1: $\sqrt{(4kTR_1)}$	$-R_2/R_1$ (Gain from input of R1 to output)
Johnson noise in R2: $\sqrt{(4kTR_2)}$	1
Inverting input current noise flowing in R2: $I_{N-} R_2$	1

Figure 1-75: Noise sources referred to the output (RTO)

Notice that the Johnson noise voltage associated with the three resistors has been included in the expressions of Figure 1-75. All resistors have a Johnson noise of  $\sqrt{4kTR}$ , where  $k$  is Boltzmann's Constant ( $1.38 \times 10^{-23}$  J/K),  $T$  is the absolute temperature,  $B$  is the bandwidth in Hz, and  $R$  is the resistance in  $\Omega$ . A simple relationship which is easy to remember is that a 1000  $\Omega$  resistor generates a Johnson noise of 4 nV/ $\sqrt{\text{Hz}}$  at 25°C.

The analysis so far assumes that the feedback network is purely resistive and that the noise gain versus frequency is flat. This applies to most applications, but if the feedback network contains reactive elements (usually capacitors) the noise gain is not constant over the bandwidth of interest, and more complex techniques must be used to calculate the total noise (see in particular, Reference 2 and Chapter 4, Section 4-4 of this book).

The circuit shown in Figure 1-76 represents a second-order system, where capacitor  $C1$  represents the source capacitance, stray capacitance on the inverting input, the input capacitance of the op amp, or any combination of these.  $C1$  causes a breakpoint in the noise gain, and  $C2$  is the capacitor that must be added to obtain stability.



**Figure 1-76: Op amp noise model with reactive elements (second-order system)**

Because of  $C1$  and  $C2$ , the noise gain is a function of frequency, and has peaking at the higher frequencies (assuming  $C2$  is selected to make the second-order system critically damped). Textbooks state that a flat noise gain can be achieved if one simply makes  $R1C1 = R2C2$ .

But in the case of current-to-voltage converters, however,  $R1$  is typically a high impedance, and the method doesn't work. Maximizing the signal bandwidth in these situations is somewhat complex and is treated in detail in Section 1-6 of this chapter and in Chapter 4, Section 4-4 of this book.

A dc signal applied to input A (B being grounded) sees a gain of  $1 + R2/R1$ , the low frequency noise gain. At higher frequencies, the gain from input A to the output becomes  $1 + C1/C2$  (the high frequency noise gain).

The closed-loop bandwidth,  $f_{cl}$ , is the point at which the noise gain intersects the open-loop gain. A dc signal applied to B (A being grounded) sees a gain of  $-R2/R1$ , with a high frequency cutoff determined by  $R2C2$ . Bandwidth from B to the output is  $1/2\pi R2C2$ .

The current noise of the noninverting input,  $I_{N+}$ , flows in  $R3$  and gives rise to a noise voltage of  $I_{N+} R3$ , which is amplified by the frequency-dependent noise gain, as are the op amp noise voltage,  $V_N$ , and the Johnson noise of  $R3$ , which is  $\sqrt{4kTR3}$ . The Johnson noise of  $R1$  is amplified by  $-R2/R1$  over a bandwidth of

$1/2\pi R2C2$ , and the Johnson noise of  $R2$  is not amplified at all but is connected directly to the output over a bandwidth of  $1/2\pi R2C2$ . The current noise of the inverting input,  $I_{N-}$ , flows in  $R2$  only, resulting in a voltage at the amplifier output of  $I_{N-}R2$  over a bandwidth of  $1/2\pi R2C2$ .

If we consider these six noise contributions, we see that if  $R1$ ,  $R2$ , and  $R3$  are low, the effect of current noise and Johnson noise will be minimized, and the dominant noise will be the op amp's voltage noise. As we increase resistance, both Johnson noise and the voltage noise produced by noise currents will rise.

If noise currents are low, Johnson noise will take over from voltage noise as the dominant contributor. Johnson noise, however, rises with the square root of the resistance, while the current noise voltage rises linearly with resistance so, ultimately, as the resistance continues to rise, the voltage due to noise currents will become dominant.

These noise contributions we have analyzed are not affected by whether the input is connected to node A or node B (the other being grounded or connected to some other low impedance voltage source), which is why the noninverting gain ( $1 + Z2/Z1$ ), which is seen by the voltage noise of the op amp,  $V_N$ , is known as the "noise gain."

Calculating the total output RMS noise of the second-order op amp system requires multiplying each of the six noise voltages by the appropriate gain and integrating over the appropriate frequency as shown in Figure 1-77.

NOISE SOURCE EXPRESSED AS A VOLTAGE	MULTIPLY BY THIS FACTOR TO REFER TO OUTPUT	INTEGRATION BANDWIDTH
Johnson noise in $R3$ : $\sqrt{4kTR3}$	Noise Gain as a function of frequency	Closed-Loop BW
Noninverting input current noise flowing in $R3$ : $I_{N+}R3$	Noise Gain as a function of frequency	Closed-Loop BW
Input voltage noise: $V_N$	Noise Gain as a function of frequency	Closed-Loop BW
Johnson noise in $R1$ : $\sqrt{4kTR1}$	$-R2/R1$ (Gain from B to output)	$1/2\pi R2C2$
Johnson noise in $R2$ : $\sqrt{4kTR2}$	1	$1/2\pi R2C2$
Inverting input current noise flowing in $R2$ : $I_{N-}R2$	1	$1/2\pi R2C2$

Figure 1-77: Noise sources referred to the output for a second-order system

The root-sum-square of all the output contributions thus represents the total RMS output noise. Fortunately, this cumbersome exercise may be greatly simplified in most cases by making the appropriate assumptions and identifying the chief contributors.

Although shown, the noise gain for a typical second-order system is repeated in Figure 1-78. It is quite easy to perform the voltage noise integration in two steps, but notice that because of peaking, the majority of the output noise due to the input voltage noise will be determined by the high frequency portion where the noise gain is  $1 + C1/C2$ . This type of response is typical of second-order systems.

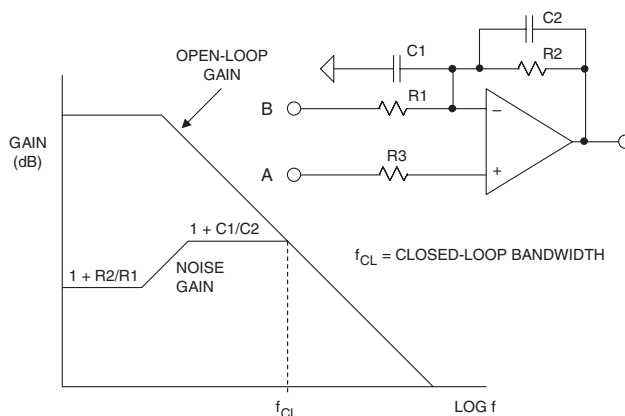


Figure 1-78: Noise gain of a typical second-order system

The noise due to the inverting input current noise,  $R1$ , and  $R2$  is only integrated over the bandwidth  $1/2\pi R2C2$ .

## Op Amp Distortion

Dynamic range of an op amp may be defined in several ways. The most common are to specify *harmonic distortion*, *total harmonic distortion* (THD), or *total harmonic distortion plus noise* (THD + N).

Other specifications related specifically to communications systems such as *intermodulation distortion* (IMD), *intercept points* (IP), *spurious free dynamic range* (SFDR), *multitone power ratio* (MTPR) and others are covered thoroughly in Chapter 6, Section 6-4. In this section, only harmonic distortion, THD, and THD + N will be covered.

The distortion components that make up total harmonic distortion are usually calculated by taking the root sum of the squares of the first five or six harmonics of the fundamental. In many practical situations, however, there is negligible error if only the second and third harmonics are included. The definition of THD and THD + N is shown in Figure 1-79.

- $V_s$  = Signal Amplitude (RMS Volts)
- $V_2$  = Second Harmonic Amplitude (RMS Volts)
- $V_n$  = nth Harmonic Amplitude (RMS Volts)
- $V_{noise}$  = RMS value of noise over measurement bandwidth

$$\bullet \quad \text{THD} + N = \frac{\sqrt{V_2^2 + V_3^2 + V_4^2 + \dots + V_n^2 + V_{noise}^2}}{V_s}$$

$$\bullet \quad \text{THD} = \frac{\sqrt{V_2^2 + V_3^2 + V_4^2 + \dots + V_n^2}}{V_s}$$

Figure 1-79: Definitions of THD and THD + N

It is important to note that the THD measurement does not include noise terms, while THD + N does. The noise in the THD + N measurement must be integrated over the measurement bandwidth. In audio applications, the bandwidth is normally chosen to be around 100 kHz. In narrow-band applications, the level of the noise may be reduced by filtering.

On the other hand, harmonics and intermodulation products which fall within the measurement bandwidth cannot be filtered, and therefore may limit the system dynamic range.

**Common-Mode Rejection Ratio (CMRR), Power Supply Rejection Ratio (PSRR)**

If a signal is applied equally to both inputs of an op amp, so that the differential input voltage is unaffected, the output should not be affected. In practice, changes in common-mode voltage will produce changes in output. The op amp *common-mode rejection ratio* (CMRR) is the ratio of the common-mode gain to differential-mode gain. For example, if a differential input change of Y volts produces a change of 1 V at the output, and a common-mode change of X volts produces a similar change of 1 V, the CMRR is X/Y. When the common-mode rejection ratio is expressed in dB, it is generally referred to as common-mode rejection (CMR). Typical LF CMR values are between 70 dB and 120 dB, but at higher frequencies CMR deteriorates. Many op amp data sheets show a plot of CMR versus frequency, as shown in Figure 1-80 for an OP177 op amp.

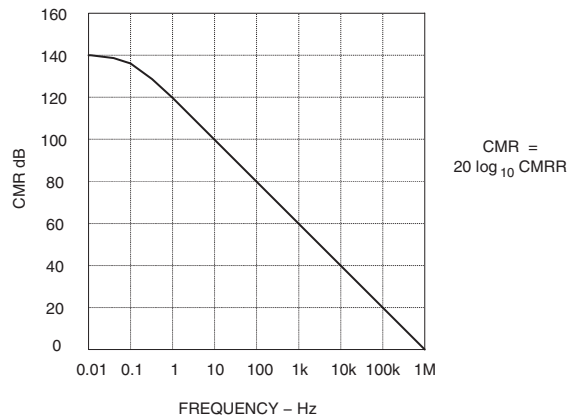
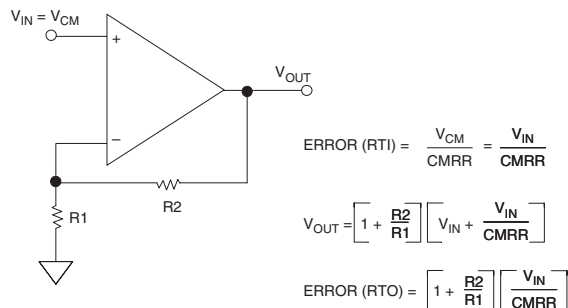


Figure 1-80: OP177 common-mode rejection (CMR)

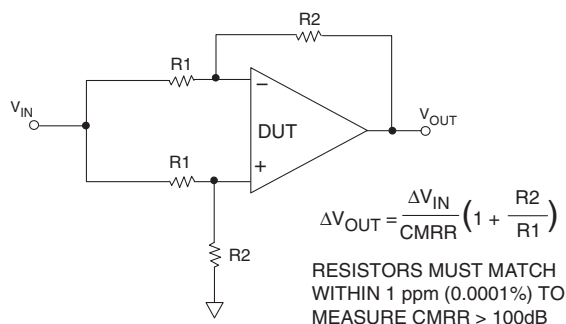
CMRR produces a corresponding output offset voltage error in op amps configured in the noninverting mode as shown in Figure 1-81.

Figure 1-81: Calculating offset error due to common-mode rejection ratio (CMRR)



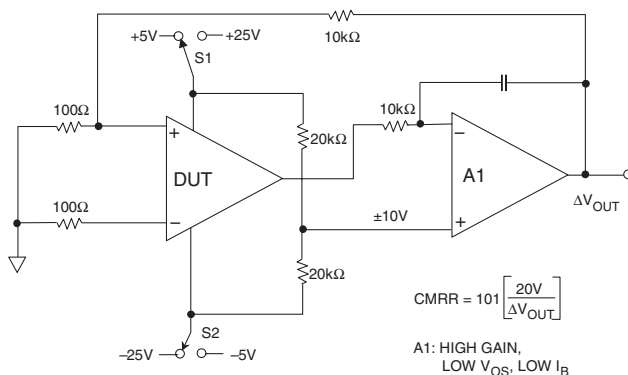
Note inverting mode operating op amps will have negligible CMRR error, as both inputs are held at a ground (or virtual ground), i.e., there is no CM dynamic voltage.

Common-mode rejection ratio can be measured in several ways. The method shown in Figure 1-82 uses four precision resistors to configure the op amp as a differential amplifier, a signal is applied to both inputs, and the change in output is measured—an amplifier with infinite CMRR would have no change in output. The disadvantage inherent in this circuit is that the ratio match of the resistors is as important as the CMRR of the op amp. A mismatch of 0.1% between resistor pairs will result in a CMR of only 66 dB—no matter how good the op amp. Since most op amps have a LF CMR of between 80 dB and 120 dB, it is clear that this circuit is only marginally useful for measuring CMRR (although it does an excellent job in measuring the matching of the resistors).



**Figure 1-82: Simple common-mode rejection ratio (CMRR) test circuit**

The slightly more complex circuit, shown in Figure 1-83, measures CMRR without requiring accurately matched resistors. In this circuit, the common-mode voltage is changed by switching the power supply voltages. (This is easy to implement in a test facility, and the same circuit with different supply voltage connections can be used to measure power supply rejection ratio.)



**Figure 1-83: CMRR test circuit does not require precision resistors**

The power supply values shown in the circuit are for a  $\pm 15$  V DUT op amp, with a common-mode voltage range of  $\pm 10$  V. Other supplies and common-mode ranges can also be accommodated by changing voltages, as appropriate. The integrating amplifier A1 should have high gain, low  $V_{OS}$ , and low  $I_B$ , such as an OP97 family device.

If the supply of an op amp changes, its output should not, but it does. The specification of *power supply rejection ratio* or PSRR is defined similarly to the definition of CMRR. If a change of X volts in the supply produces the same output change as a differential input change of Y volts, the PSRR on that supply is X/Y. The definition of PSRR assumes that both supplies are altered equally in opposite directions—otherwise the change will introduce a common-mode change as well as a supply change, and the analysis becomes considerably more complex. It is this effect that causes apparent differences in PSRR between the positive and negative supplies.

Typical PSR for the OP177 is shown in Figure 1-84.

The test setup used to measure CMRR may be modified to measure PSRR as shown in Figure 1-85.

The voltages are chosen for a symmetrical power supply change of 1 V. Other values may be used where appropriate.

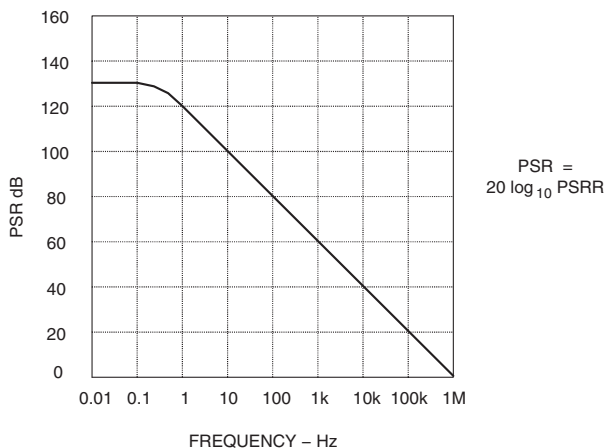


Figure 1-84: OP177 power supply rejection

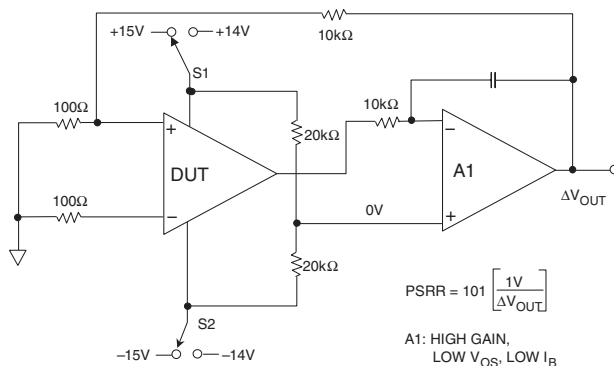
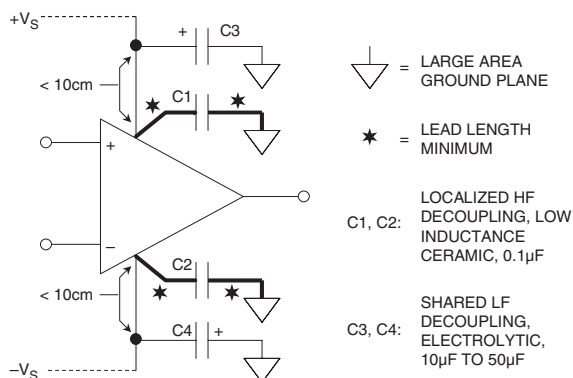


Figure 1-85: Test setup for measuring power supply rejection ratio (PSRR)

## Power Supplies and Decoupling

Because op amp PSRR is frequency dependent, op amp power supplies must be well decoupled. At low frequencies, several devices may share a 10  $\mu\text{F}$ –50  $\mu\text{F}$  capacitor on each supply, provided it is no more than 10cm (PC track distance) from any of them.

At high frequencies, each IC should have the supply leads decoupled by a low inductance 0.1  $\mu\text{F}$  (or so) capacitor with short leads/PC tracks. These capacitors must also provide a return path for HF currents in the op amp load. Typical decoupling circuits are shown in Figure 1-86. Further bypassing and decoupling information is found Chapter 7.



**Figure 1-86: Proper low and high-frequency decoupling techniques for op amps**

## Power Supplies and Power Dissipation

Op amps have no ground terminal. Specifications of power supply are quite often in the form  $\pm X$  Volts, but in fact it might equally be expressed as  $2X$  Volts. What is important is where the CM and output ranges lie relative to the supplies. This information may be provided in tabular form or as a graph.

Data sheets will often advise that an op amp will work over a range of supplies (from +3 V to  $\pm 16.5$  V for example), and will then give parameters at several values of supply, so that users may extrapolate. If the minimum supply is quite high, it is usually because the device uses a structure requiring a threshold voltage to function (zener diode).

Data sheets also give current consumption. Any current flowing into one supply pin will flow out of the other or out of the output terminal. When the output is open circuit, the dissipation is easily calculated from the supply voltage and current. When current flows in a load, it is easiest to calculate the total dissipation (remember that if the load is grounded to the center rail the load current flows from a supply to ground, not between supplies), and then subtract the load dissipation to obtain the device dissipation. Data sheets normally give details of thermal resistances and maximum junction temperature ratings, from which dissipation limits may be calculated knowing conditions. Details of further considerations relating to power dissipation, heatsinking, and so forth, can be found in Chapter 7, Section 7-5.



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## Precision Op Amps

*Walt Kester, Walt Jung*

This section examines in more detail some of the issues relating to amplifiers for use in precision signal conditioning applications. Although the OP177 op amp is used for the “gold standard” for precision in these discussions, more recent product introductions such as the rail-to-rail output OP777, OP727, and OP747, along with the OP1177, OP2177, and OP4177 offer nearly as good performance in smaller packages.

Precision op amp open-loop gains greater than 1 million are available, along with common-mode and power supply rejection ratios of the same magnitude. Offset voltages of less than 25  $\mu\text{V}$  and offset drift less than 0.1  $\mu\text{V}/^\circ\text{C}$  are available in dual supply op amps such as the OP177, however, the performance in single-supply precision bipolar op amps may sometimes fall short of this performance. This is the trade-off that must sometimes be made in low power, low voltage applications. On the other hand, however, modern chopper stabilized op amps provide offsets and offset voltage drifts which cannot be distinguished from noise, and these devices operate on single supplies and provide rail-to-rail inputs and outputs. They, too, come with their own set of problems that are discussed later within this section.

It is important to understand that dc open-loop gain, offset voltage, power supply rejection (PSR), and common-mode rejection (CMR) alone shouldn't be the only considerations in selecting precision amplifiers. The ac performance of the amplifier is also important, even at “low” frequencies. Open-loop gain, PSR, and CMR all have relatively low corner frequencies; therefore, what may be considered “low” frequency may actually fall above these corner frequencies, increasing errors above the value predicted solely by the dc parameters. For example, an amplifier having a dc open-loop gain of 10 million and a unity-gain crossover frequency of 1 MHz has a corresponding corner frequency of 0.1 Hz. One must therefore consider the open-loop gain at the actual *signal* frequency. The relationship between the single-pole unity-gain crossover frequency,  $f_u$ , the signal frequency,  $f_{\text{sig}}$ , and the open-loop gain  $A_{\text{VOL}(f_{\text{sig}})}$  (measured at the signal frequency) is given by:

$$A_{\text{VOL}(f_{\text{sig}})} = \frac{f_u}{f_{\text{sig}}} \quad \text{Eq. 1-31}$$

In the example above, the open-loop gain is 10 at 100 kHz, and 100,000 at 10 Hz. Note that the constant gain-bandwidth product concept only holds true for VFB op amps. It doesn't apply to CFB op amps, but then they are rarely used in precision applications.

Loss of open-loop gain at the frequency of interest can introduce distortion, especially at audio frequencies. Loss of CMR or PSR at the line frequency or harmonics thereof can also introduce errors.

The challenge of selecting the right amplifier for a particular signal conditioning application has been complicated by the sheer proliferation of various types of amplifiers in various processes (Bipolar, Complementary Bipolar, BiFET, CMOS, BiCMOS, and so forth) and architectures (traditional op amps, instrumentation amplifiers, chopper amplifiers, isolation amplifiers, and so forth)

In addition, a wide selection of precision amplifiers which operate on single-supply voltages are now available which complicates the design process even further because of the reduced signal swings and voltage input and output restrictions. Offset voltage and noise are now a more significant portion of the input signal.

Selection guides and parametric search engines, which can simplify this process somewhat, are available on the World Wide Web ([www.analog.com](http://www.analog.com)) as well as on CDROM. Some general attributes of precision op amps are summarized in Figure 1-87.

- Input Offset Voltage <100μV
- Input Offset Voltage Drift <1μV/°C
- Input Bias Current <2nA
- Input Offset Current <2nA
- DC Open-Loop Gain >1,000,000
- Unity Gain Bandwidth Product,  $f_u$  500kHz – 5MHz
- Always Check Open Loop Gain at Signal Frequency
- 1/f (0.1Hz to 10Hz) Noise <1μV p-p
- Wideband Noise <10nV/ $\sqrt{\text{Hz}}$
- CMR, PSR >100dB
- Trade-offs:
  - Single supply operation
  - Low supply currents

Figure 1-87: Precision op amp characteristics

Precision Op Amp Amplifier DC Error Budget Analysis

In order to develop a concept for the magnitudes of the various errors in a high precision op amp circuit, a simple room temperature analysis for the OP177F is shown in Figure 1-88. The amplifier is connected in the inverting mode with a signal gain of 100. The key data sheet specifications are also shown in the diagram. We assume an input signal of 100 mV fullscale which corresponds to an output signal of 10 V. The various error sources are normalized to full-scale and expressed in parts per million (ppm). Note: parts per million (ppm) error = fractional error  $\times 10^6 = \% \text{ error} \times 10^4$ .

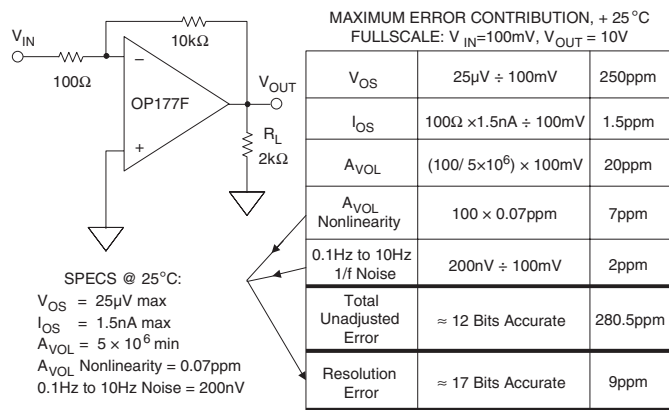


Figure 1-88: Precision op amp (OP177F) dc error budget analysis

Note that the offset errors due to  $V_{OS}$  and  $I_{OS}$  and the gain error due to finite  $A_{VOL}$  can be removed with a system calibration. However, the error due to open-loop gain nonlinearity cannot be removed with calibration and produces a relative accuracy error, often called *resolution error*.

A second contributor to resolution error is the  $1/f$  noise. This noise is always present and adds to the uncertainty of the measurement. The overall relative accuracy of the circuit at room temperature is 9ppm, equivalent to  $\sim 17$  bits of resolution.

It is also useful to compare the performance of a number of single-supply op amps to that of the “gold standard” OP177, and this is done in Figure 1-89 for some representative devices.

Note that the Figure 1-89 amplifier list does *not* include the category of chopper op amps, which excel in many of the categories. These are covered separately, next.

LISTED IN ORDER OF INCREASING SUPPLY CURRENT							
PART NO.	$V_{OS\ max}$	$V_{OS\ TC}$	$A_{VOL\ min}$	NOISE (1kHz)	INPUT	OUTPUT	$I_{SY/AMP\ MAX}$
OP293	250 $\mu$ V	2 $\mu$ V/ $^{\circ}$ C	200k	5nV/ $\sqrt{Hz}$	0, 4V	5mV, 4V	20 $\mu$ A
OP196/296/496	300 $\mu$ V	2 $\mu$ V/ $^{\circ}$ C	150k	26nV/ $\sqrt{Hz}$	R/R	“R/R”	60 $\mu$ A
OP777	100 $\mu$ V	1.3 $\mu$ V/ $^{\circ}$ C	300k	15nV/ $\sqrt{Hz}$	0, 4V	“R/R”	270 $\mu$ A
OP191/291/491	700 $\mu$ V	5 $\mu$ V/ $^{\circ}$ C	25k	35nV/ $\sqrt{Hz}$	R/R	“R/R”	350 $\mu$ A
*AD820/822/824	1000 $\mu$ V	20 $\mu$ V/ $^{\circ}$ C	500k	16nV/ $\sqrt{Hz}$	0, 4V	“R/R”	800 $\mu$ A
**AD8601/2/4	600 $\mu$ V	2 $\mu$ V/ $^{\circ}$ C	20k	33nV/ $\sqrt{Hz}$	R/R	“R/R”	1000 $\mu$ A
OP184/284/484	150 $\mu$ V	2 $\mu$ V/ $^{\circ}$ C	50k	3.9nV/ $\sqrt{Hz}$	R/R	“R/R”	1350 $\mu$ A
OP113/213/413	175 $\mu$ V	4 $\mu$ V/ $^{\circ}$ C	2M	4.7nV/ $\sqrt{Hz}$	0, 4V	5mV, 4V	3000 $\mu$ A
OP177F ( $\pm 15$ V)	25 $\mu$ V	0.1 $\mu$ V/ $^{\circ}$ C	5M	10nV/ $\sqrt{Hz}$	N/A	N/A	2000 $\mu$ A

\*JFET INPUT    \*\*CMOS    NOTE: Unless Otherwise Stated  
Specifications are Typical @ 25 $^{\circ}$ C  
 $V_S = 5$ V

**Figure 1-89: Precision single-supply op amp performance characteristics**

## Chopper Stabilized Amplifiers

For the lowest offset and drift performance, chopper-stabilized amplifiers may be the only solution. The best bipolar amplifiers offer offset voltages of  $25\ \mu\text{V}$  and  $0.1\ \mu\text{V}/^\circ\text{C}$  drift. Offset voltages less than  $5\ \mu\text{V}$  with practically no measurable offset drift are obtainable with choppers, albeit with some penalties.

A basic chopper amplifier circuit is shown in Figure 1-90. When the switches are in the “Z” (auto-zero) position, capacitors C2 and C3 are charged to the amplifier input and output offset voltage, respectively. When the switches are in the “S” (sample) position,  $V_{\text{IN}}$  is connected to  $V_{\text{OUT}}$  through the path comprised of R1, R2, C2, the amplifier, C3, and R3. The chopping frequency is usually between a few hundred Hz and several kHz, and it should be noted that because this is a sampling system, the input frequency must be much less than one-half the chopping frequency in order to prevent errors due to aliasing. The R1-C1 combination serves as an antialiasing filter. It is also assumed that after a steady state condition is reached, there is only a minimal amount of charge transferred during the switching cycles. The output capacitor, C4, and the load,  $R_L$ , must be chosen such that there is minimal  $V_{\text{OUT}}$  droop during the auto-zero cycle.

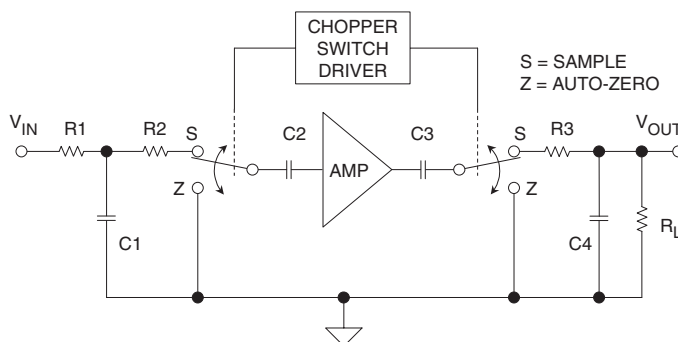


Figure 1-90: Classic chopper amplifier

The basic chopper amplifier of Figure 1-90 can pass only very low frequencies because of the input filtering required to prevent aliasing. In contrast to this, the *chopper-stabilized* architecture shown in Figure 1-91 is most often used in chopper amplifier implementations. In this circuit, A1 is the *main* amplifier, and A2 is

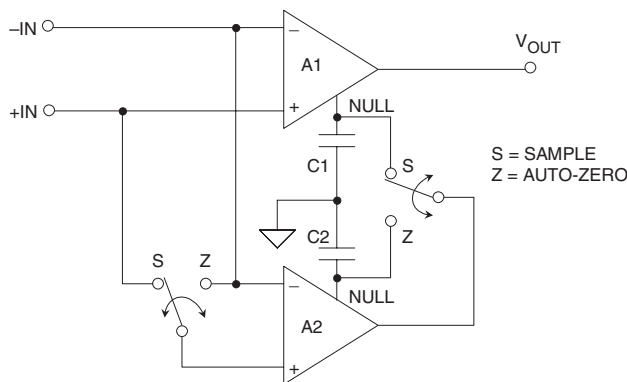


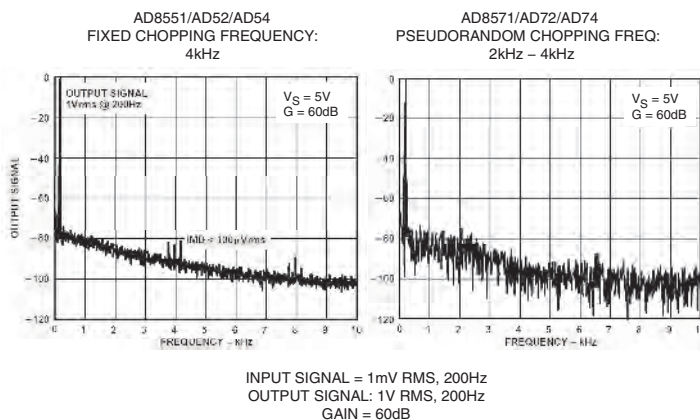
Figure 1-91: Modern chopper stabilized op amp

the *nulling* amplifier. In the sample mode (switches in “S” position), the nulling amplifier, A2, monitors the input offset voltage of A1 and drives its output to zero by applying a suitable correcting voltage at A1’s null pin. Note, however, that A2 also has an input offset voltage, so it must correct its own error before attempting to null A1’s offset. This is achieved in the auto-zero mode (switches in “Z” position) by momentarily disconnecting A2 from A1, shorting its inputs together, and coupling its output to its own null pin. During the auto-zero mode, the correction voltage for A1 is momentarily held by C1. Similarly, C2 holds the correction voltage for A2 during the sample mode. In modern IC chopper-stabilized op amps, the storage capacitors C1 and C2 are on-chip.

Note in this architecture that *the input signal is always connected to the output, through A1*. The bandwidth of A1 thus determines the overall signal bandwidth, and the input signal is not limited to less than one-half the chopping frequency as in the case of the traditional chopper amplifier architecture. However, the switching action does produce small transients at the chopping frequency, which can mix with the input signal frequency and produce intermodulation distortion.

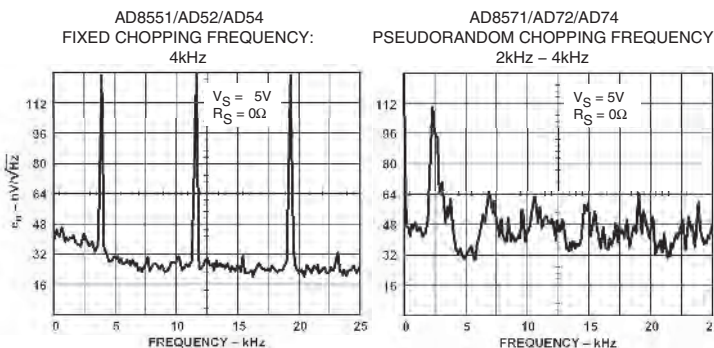
A patented spread-spectrum technique is used in the AD8571/AD72/AD74 series of single-supply chopper-stabilized op amps, to virtually eliminate intermodulation effects.

These devices use a pseudorandom chopping frequency swept between 2 kHz and 4 kHz. Figure 1-92 compares the intermodulation distortion of a traditional chopper stabilized op amp (AD8551/AD52/AD54, left) that uses a fixed 4 kHz chopping frequency to that of the AD8571/AD72/AD74 (right) that uses the pseudorandom chopping frequency.



**Figure 1-92: Intermodulation product:  
fixed pseudorandom chopping frequency**

A comparison between fixed and pseudorandom chopping on the voltage noise is shown in Figure 1-93. Notice for the fixed chopping frequency, there are distinct peaks in the noise spectrum at the odd harmonics of 4 kHz, whereas with pseudorandom chopping, the spectrum is much more uniform, although the average noise level is higher.



**Figure 1-93: Voltage noise spectral density comparison: fixed versus pseudorandom chopping frequency**

The AD8571/AD8572/AD8574 family of chopper-stabilized op amps offers rail-to-rail input and output single-supply operation, low offset voltage, and low offset drift. As discussed above, the pseudorandom chopping frequency minimizes intermodulation distortion with the input signal. The storage capacitors are internal to the IC, and no external capacitors other than standard decoupling capacitors are required. Key specifications for the devices are given in Figure 1-94.

- Single Supply: 2.7V to 5V
- 1μV Typical Input Offset Voltage
- 0.005μV/°C Typical Input Offset Voltage Drift
- 130dB CMR, PSR
- 750μA Supply Current/Op Amp
- 50μs Overload Recovery Time
- 50nV/√Hz Input Voltage Noise
- Pseudorandom Chopping Frequency
- 1.5MHz Gain-Bandwidth Product
- Single (AD8571), Dual (AD8572) and Quad (AD8574)

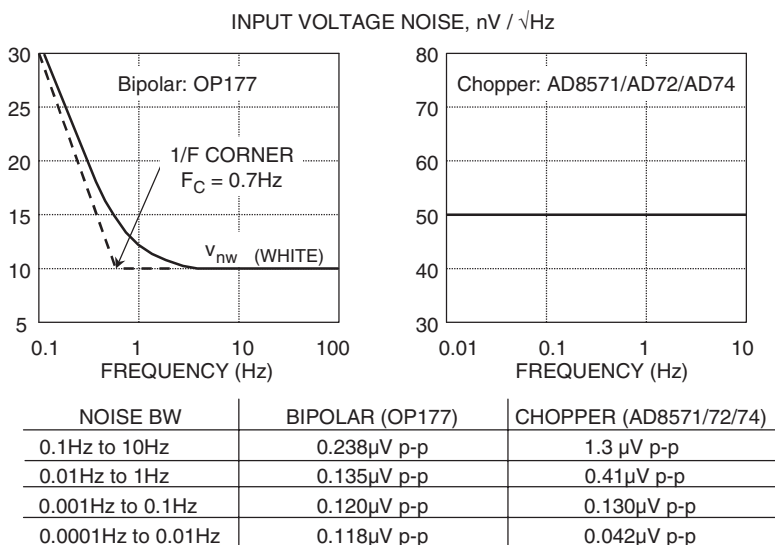
**Figure 1-94: AD8571/AD72/AD74 chopper-stabilized rail-to-rail input/output amplifiers**

It should be noted that extreme care must be taken when applying all of the chopper-stabilized devices. This is because in order to fully realize the full offset and drift performance inherent to the parts, parasitic thermocouple effects in external circuitry must be avoided. See Chapter 4, Section 4-5 for a general discussion of thermocouples, and Chapter 7, Section 7-1 related to passive components.

## Noise Considerations for Chopper-Stabilized Op Amps

It is interesting to consider the effects of a chopper amplifier on low frequency  $1/f$  noise. If the chopping frequency is considerably higher than the  $1/f$  corner frequency of the input noise, the chopper-stabilized amplifier continuously nulls out the  $1/f$  noise on a sample-by-sample basis. Theoretically, a chopper op amp therefore has no  $1/f$  noise. However, the chopping action produces wideband noise which is generally much worse than that of a precision bipolar op amp.

Figure 1-95 shows the noise of a precision bipolar amplifier (OP177) versus that of the AD8571/AD72/AD74 chopper-stabilized op amp. The peak-to-peak noise in various bandwidths is calculated for each in the table below the graphs.



**Figure 1-95: Noise: bipolar versus chopper stabilized op amp**

Note from the data that as the frequency is lowered, the chopper amplifier noise continues to drop, while the bipolar amplifier noise approaches a limit determined by the  $1/f$  corner frequency and its white noise. Notice that only at very low frequencies ( $<0.01$  Hz) is the chopper noise performance superior to that of the bipolar op amp.

In order to take advantage of the chopper op amp's lack of  $1/f$  noise, much filtering is required—otherwise the total noise of a chopper will always be worse than a good bipolar op amp. Choppers should therefore be selected on the basis of their low offset and drift—not because of their lack of  $1/f$  noise.



**References: Precision Op Amps**

1. Walt Kester, Editor, **1992 Amplifier Applications Guide**, Analog Devices, 1992, ISBN: 0-916550-10-9.
2. Walt Kester, Editor, **Practical Design Techniques for Sensor Signal Conditioning**, Analog Devices, 1999, ISBN: 0-916550-20-6.
3. Data Sheet for **AD8551/AD8552/AD8554 Zero-Drift, Single-Supply, Rail-to-Rail Input/Output Operational Amplifiers**, at [www.analog.com](http://www.analog.com).
4. Data Sheet for **AD8571/AD8572/AD8574 Zero-Drift, Single-Supply, Rail-to-Rail Input/Output Operational Amplifiers**, at [www.analog.com](http://www.analog.com).
5. Data Sheet for **OP777/OP727/OP747 Precision Micropower Single-Supply Operational Amplifiers**, at [www.analog.com](http://www.analog.com).
6. Data Sheet for **OP1177/OP2177/OP4177 Precision Low Noise, Low Input Bias Current Operational Amplifiers**, at [www.analog.com](http://www.analog.com).

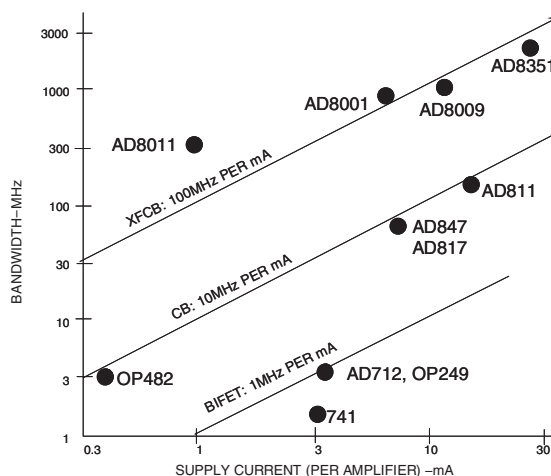
# High Speed Op Amps

Walt Kester

## Introduction

High speed analog signal processing applications, such as video and communications, require op amps that have wide bandwidth, fast settling time, low distortion and noise, high output current, good dc performance, and operate at low supply voltages. These devices are widely used as gain blocks, cable drivers, ADC pre-amps, current-to-voltage converters, and so forth. Achieving higher bandwidths for less power is extremely critical in today's portable and battery-operated communications equipment. The rapid progress made over the last few years in high speed linear circuits has hinged not only on the development of IC processes but also on innovative circuit topologies.

The evolution of high speed processes using amplifier bandwidth as a function of supply current as a figure of merit is shown in Figure 1-96. (In the case of duals, triples, and quads, the current per amplifier is used.) Analog Devices BiFET process, which produced the AD712 (3 MHz bandwidth, 3 mA current) yields about 1 MHz per mA.



**Figure 1-96: Amplifier bandwidth versus supply current for Analog Devices' processes**

The CB (Complementary Bipolar) process (AD817, AD847, AD811, and so forth) yields about 10 MHz/mA of supply current. The  $f_s$  of the CB process PNP transistors are about 700 MHz, and the NPNs about 900 MHz. The CB process at Analog Devices was introduced in 1985.

The next complementary bipolar process from Analog Devices was a high speed dielectrically isolated process called "XFCB" (eXtra Fast Complementary Bipolar) which was introduced in 1992. This process yields 3 GHz PNPs and 5 GHz matching NPNs, and coupled with innovative circuit topologies allows

op amps to achieve new levels of cost-effective performance at astonishing low quiescent currents. The approximate figure of merit for this process is typically 100 MHz/mA, although the AD8011 op amp is capable of 300 MHz bandwidth on 1 mA of supply current due to its unique two-stage current-feedback architecture described later in this section.

Even faster CB processes have been developed at Analog Devices for low voltage supply products such as “XFCB 1.5” (5 GHz PNP, 9 GHz NPN), and “XFCB 2” (9 GHz PNP, 16 GHz NPN). The AD8351 differential low distortion RF amplifier (shown on Figure 1-96) is fabricated on “XFCB 1.5” and has a bandwidth of 2 GHz for a gain of 12 dB. It is expected that newer complementary bipolar processes will be optimized for higher  $f_s$ .

In order to select intelligently the correct high speed op amp for a given application, an understanding of the various op amp topologies as well as the trade-offs between them is required. The two most widely used topologies are voltage feedback (VFB) and current feedback (CFB). An overview of these topologies has been presented in a previous section, but the following discussion treats the frequency-related aspects of the two topologies in considerably more detail.

## Voltage Feedback (VFB) Op Amps

A voltage feedback (VFB) op amp is distinguished from a current feedback (CFB) op amp by circuit topology. The VFB op amp is certainly the most popular in low frequency applications, but the CFB op amp has some advantages at high frequencies. We will discuss CFB in detail later, but first the more traditional VFB architecture.

Early IC voltage feedback op amps were made on “all NPN” processes. These processes were optimized for NPN transistors—the “lateral” PNP transistors had relatively poor performance. Some examples of these early VFB op amps using these poor quality PNPs include the 709, the LM101 and the 741 (see Chapter 8: “Op Amp History”).

Lateral PNPs were generally used only as current sources, level shifters, or for other noncritical functions. A simplified diagram of a typical VFB op amp manufactured on such a process is shown in Figure 1-97.

The input stage is a differential pair (sometimes called a *long-tailed pair*) consisting of either a bipolar pair (Q1, Q2) or a FET pair. This “ $g_m$ ” (transconductance) stage converts the small-signal differential input

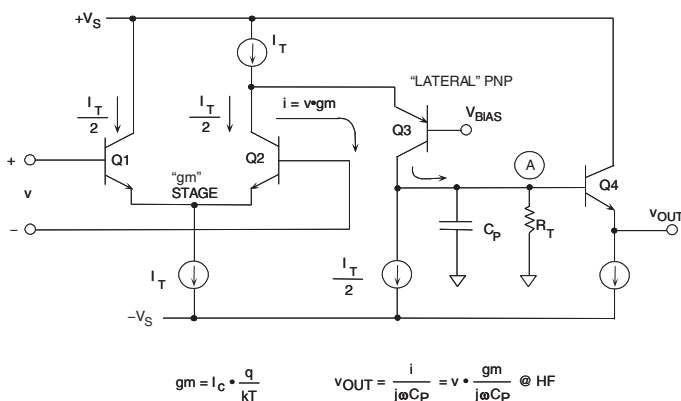


Figure 1-97: Voltage feedback (VFB) op amp designed on an “all NPN” IC process

voltage,  $v$ , into a current,  $i$ , and its transfer function is measured in units of conductance,  $1/\Omega$ , (or mhos). The small-signal emitter resistance,  $r_e$ , is approximately equal to the reciprocal of the small-signal  $g_m$ .

The formula for the small-signal  $g_m$  of a single bipolar transistor is given by the following equation:

$$g_m = \frac{1}{r_e} = \frac{q}{kT} (I_C) = \frac{q}{kT} \left( \frac{I_T}{2} \right), \text{ or} \quad \text{Eq. 1-32}$$

$$g_m \approx \left( \frac{1}{26\text{mV}} \right) \left( \frac{I_T}{2} \right). \quad \text{Eq. 1-33}$$

where  $I_T$  is the differential pair tail current,  $I_C$  is the collector quiescent bias current ( $I_C = I_T/2$ ),  $q$  is the electron charge,  $k$  is Boltzmann's constant, and  $T$  is absolute temperature. At  $25^\circ\text{C}$ ,  $V_T = kT/q = 26 \text{ mV}$  (often called the *thermal voltage*,  $V_T$ ).

As we will see shortly, the amplifier unity gain-bandwidth product,  $f_u$ , is equal to  $g_m/2\pi C_p$ , where the capacitance  $C_p$  is used to set the dominant pole frequency. For this reason, the tail current,  $I_T$ , is made proportional to absolute temperature (PTAT). This current tracks the variation in  $r_e$  with temperature thereby making  $g_m$  independent of temperature. It is relatively easy to make  $C_p$  reasonably constant over temperature.

The Q2 collector output of the  $g_m$  stage drives the emitter of a lateral PNP transistor (Q3). It is important to note that Q3 is not used to amplify the signal, only to level shift, i.e., the signal current variation in the collector of Q2 appears at the collector of Q3. The collector current of Q3 develops a voltage across high impedance node A, and  $C_p$  sets the dominant pole of the amplifier. Emitter follower Q4 provides a low impedance output.

The effective load at the high impedance node A can be represented by a resistance,  $R_T$ , in parallel with the dominant pole capacitance,  $C_p$ . The small-signal output voltage,  $v_{out}$ , is equal to the small-signal current,  $i$ , multiplied by the impedance of the parallel combination of  $R_T$  and  $C_p$ .

Figure 1-98 shows a simple model for the single-stage amplifier and the corresponding Bode plot. The Bode plot is conveniently constructed on a log-log scale.

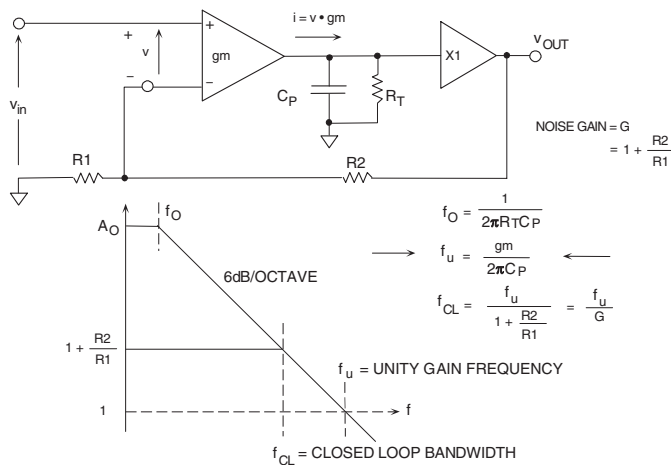


Figure 1-98: Model and Bode plot for a VFB op amp

The low frequency breakpoint,  $f_o$ , is given by:

$$f_o = \frac{1}{2\pi R_T C_p} \quad \text{Eq. 1-34}$$

Note that the high frequency response is determined solely by  $g_m$  and  $C_p$ :

$$v_{out} = v \cdot \frac{g_m}{j\omega C_p} \quad \text{Eq. 1-35}$$

The unity gain bandwidth frequency,  $f_u$ , occurs where  $|v_{out}| = |v|$ . Letting  $\omega = 2\pi f_u$  and  $|v_{out}| = |v|$ , Eq. 1-35 can be solved for  $f_u$ ,

$$f_u = \frac{g_m}{2\pi C_p} \quad \text{Eq. 1-36}$$

We can use feedback theory to derive the closed-loop relationship between the circuit's signal input voltage,  $v_{in}$ , and its output voltage,  $v_{out}$ :

$$\frac{v_{out}}{v_{in}} = \frac{1 + \frac{R2}{R1}}{1 + \frac{j\omega C_p}{g_m} \left(1 + \frac{R2}{R1}\right)} \quad \text{Eq. 1-37}$$

At the op amp 3 dB closed-loop bandwidth frequency,  $f_{cl}$ , the following is true:

$$\frac{2\pi f_{cl} C_p}{g_m} \left(1 + \frac{R2}{R1}\right) = 1, \text{ and hence} \quad \text{Eq. 1-38}$$

$$f_{cl} = \frac{g_m}{2\pi C_p} \left( \frac{1}{1 + \frac{R2}{R1}} \right), \text{ or} \quad \text{Eq. 1-39}$$

$$f_{cl} = \frac{f_u}{1 + \frac{R2}{R1}} \quad \text{Eq. 1-40}$$

This demonstrates the fundamental property of VFB op amps: *The closed-loop bandwidth multiplied by the closed-loop gain is a constant*, i.e., the VFB op amp exhibits a constant gain-bandwidth product over most of the usable frequency range.

As noted previously, some VFB op amps (called *decompensated*) are not stable at unity gain, but designed to be operated at some minimum (higher) amount of closed-loop gain. However, even for these op amps, the gain bandwidth product is still relatively constant over the region of stability.

Now, consider the following typical example:  $I_T = 100 \mu A$ ,  $C_p = 2 \text{ pF}$ . We find that:

$$g_m = \frac{I_T / 2}{V_T} = \frac{50 \mu A}{26 \text{ mV}} = \frac{1}{520 \Omega} \quad \text{Eq. 1-41}$$

$$f_u = \frac{g_m}{2\pi C_p} = \frac{1}{2\pi(520)(2 \cdot 10^{-12})} = 153 \text{ MHz} \quad \text{Eq. 1-42}$$

Now, we must consider the large-signal response of the circuit. The slew-rate, SR, is simply the total available charging current,  $I_T/2$ , divided by the dominant pole capacitance,  $C_p$ . For the example under consideration,

$$I = C \frac{dv}{dt}, \frac{dv}{dt} = \text{SR}, \text{SR} = \frac{I}{C} \quad \text{Eq. 1-43}$$

$$\text{SR} = \frac{I_T/2}{C_p} = \frac{50 \mu\text{A}}{2 \text{ pF}} = 25 \text{ V}/\mu\text{s} \quad \text{Eq. 1-44}$$

The full-power bandwidth (FPBW) of the op amp can now be calculated from the formula:

$$\text{FPBW} = \frac{\text{SR}}{2\pi A} = \frac{25 \text{ V}/\mu\text{s}}{2\pi \cdot 1\text{V}} = 4 \text{ MHz} \quad \text{Eq. 1-45}$$

where  $A$  is the peak amplitude of the output signal. If we assume a 2 V peak-to-peak output sinewave (certainly a reasonable assumption for high speed applications), then we obtain a FPBW of only 4 MHz, even though the small-signal unity gain bandwidth product is 153 MHz. For a 2 V p-p output sinewave, distortion will begin to occur much lower than the actual FPBW frequency. We must increase the SR by a factor of about 40 in order for the FPBW to equal 153 MHz. The only way to do this is to increase the tail current,  $I_T$ , of the input differential pair by the same factor. This implies a bias current of 4 mA in order to achieve a FPBW of 160 MHz. We are assuming that  $C_p$  is a fixed value of 2 pF and cannot be lowered by design. These calculations are summarized in Figure 1-99.

- Assume that  $I_T = 100 \mu\text{A}$ ,  $C_p = 2 \text{ pF}$ 

$$g_m = \frac{I_C}{V_T} = \frac{50 \mu\text{A}}{26 \text{ mV}} = \frac{1}{520 \Omega}$$

$$f_u = \frac{g_m}{2\pi C_p} = 153 \text{ MHz}$$
- Slew Rate = SR =  
But for 2V peak-peak output ( $A = 1\text{V}$ )
 
$$\text{FPBW} = \frac{\text{SR}}{2\pi A} = 4 \text{ MHz}$$
- Must increase  $I_T$  to 4mA to get FPBW = 160MHz
- Reduce  $g_m$  by adding emitter degeneration resistors

**Figure 1-99: VFB op amp bandwidth and slew rate calculations**

In practice, the FPBW of the op amp should be approximately 5 to 10 times the maximum output frequency in order to achieve acceptable distortion performance (typically 55 dBc–80 dBc @ 5 MHz to 20 MHz, but actual system requirements vary widely).

Notice, however, that increasing the tail current causes a proportional increase in  $g_m$  and hence  $f_u$ . In order to prevent possible instability due to the large increase in  $f_u$ ,  $g_m$  can be reduced by inserting resistors in

series with the emitters of Q1 and Q2 (this technique, called *emitter degeneration*, also serves to linearize the  $g_m$  transfer function and thus also lowers distortion).

This analysis points out that a major inefficiency of conventional bipolar voltage feedback op amps is their inability to achieve high slew rates without proportional increases in quiescent current (assuming that  $C_p$  is fixed, and has a reasonable minimum value of 2 pF or 3 pF).

This of course is not meant to say that high speed op amps designed using this architecture are deficient, just that circuit design techniques are available that allow equivalent performance at much lower quiescent currents. This is extremely important in portable battery-operated equipment where every milliwatt of power dissipation is critical.

### VFB Op Amps Designed on Complementary Bipolar Processes

With the advent of complementary bipolar (CB) processes having high quality PNP transistors as well as NPNs, VFB op amp configurations such as the one shown in the simplified diagram in Figure 1-100 became popular.

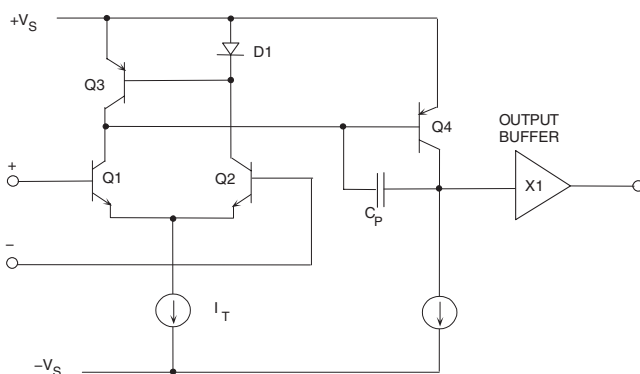


Figure 1-100: VFB op amp using two gain stages

Notice that the input differential pair (Q1, Q2) is loaded by a current mirror (Q3 and D1). We show D1 as a diode for simplicity, but it is actually a diode-connected PNP transistor (matched to Q3) with the base and collector connected to each other. This simplification will be used in many of the circuit diagrams to follow in this section. The common emitter transistor, Q4, provides a *second* voltage gain stage.

Since the PNP transistors are fabricated on a complementary bipolar process, they are high quality and matched to the NPNs, and therefore suitable for voltage gain. The dominant pole of the Figure 1-100 amplifier is set by  $C_p$ , and the combination of the gain stage, Q4, and local feedback capacitor  $C_p$  is often referred to as a *Miller Integrator*. The unity gain output buffer is usually a complementary emitter follower.

A model for this two-stage VFB op amp is shown in Figure 1-101. Notice that the unity gain bandwidth frequency,  $f_u$ , is still determined by the input stage  $g_m$  and the dominant pole capacitance,  $C_p$ . The second gain stage increases the dc open-loop gain, but maximum slew rate is still limited by the input stage tail current as:  $SR = I_T/C_p$ .

A two-stage amplifier topology such as this is widely used throughout the IC industry in VFB op amps, both precision and high speed. It can be recalled that a similar topology with a dual FET input stage was used in the early high speed, fast settling FET modular op amps (see Chapter 8: “Op Amp History”).

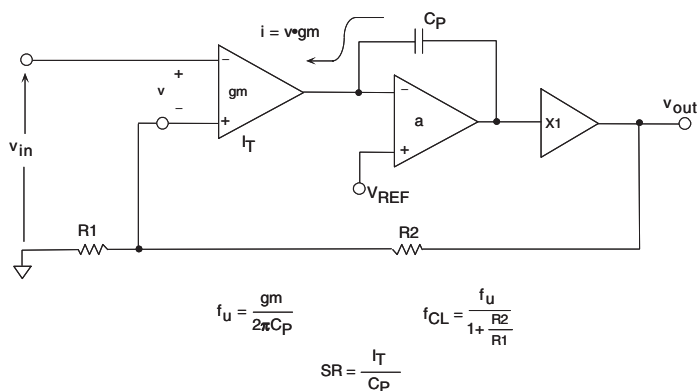


Figure 1-101: Model for two stage VFB op amp

Another popular VFB op amp architecture is the *folded cascode* as shown in Figure 1-102. An industry-standard video amplifier family (the AD847) is based on this architecture. This circuit also takes advantage of the fast PNPs available on a CB process. The differential signal currents in the collectors of Q1 and Q2 are fed to the emitters of a PNP cascode transistor pair (hence the term *folded cascode*). The collectors of Q3 and Q4 are loaded with the current mirror, D1 and Q5, and voltage gain is developed at the Q4–Q5 node. This single-stage architecture uses the junction capacitance at the high impedance node for compensation ( $C_{STRAY}$ ). Some variations of the design bring this node to an external pin so that additional external capacitance can be added if desired.

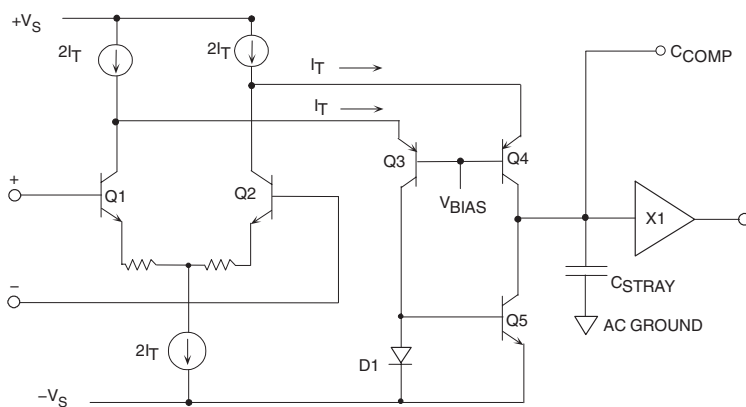


Figure 1-102: AD847 family folded cascode simplified circuit

With no emitter degeneration resistors in Q1 and Q2, and no additional external compensating capacitance, this circuit is only stable for high closed-loop gains. However, unity gain compensated versions of this family are available with the appropriate amount of emitter degeneration.



The availability of JFETs on a CB process allows not only low input bias current but also improvements in the slew rate trade-off, which must be made between  $g_m$  and  $I_T$  found in bipolar input stages. Figure 1-103 shows a simplified diagram of the AD845 16 MHz op amp. JFETs have a much lower  $g_m$  per mA of tail current than a bipolar transistor. This lower  $g_m$  of the FET allows the input tail current (hence the slew rate) to be increased, without having to increase  $C_p$  to maintain stability.

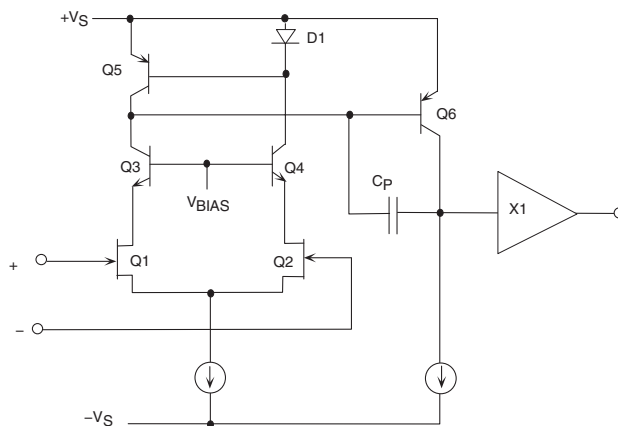


Figure 1-103: AD845 BiFET 16 MHz op amp simplified circuit

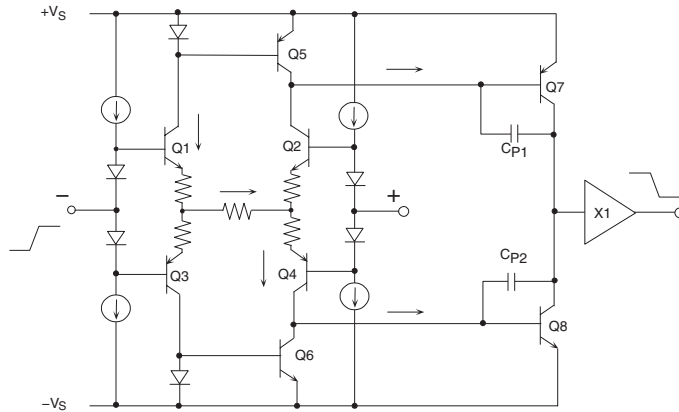
The unusual thing about this seemingly poor performance of the JFET is that it is exactly what is needed for a fast, high SR input stage. For a typical JFET, the value of  $g_m$  is approximately  $I_s/1\text{ V}$  ( $I_s$  is the source current), rather than  $I_c/26\text{ mV}$  for a bipolar transistor, i.e., the FET  $g_m$  is about 40 times lower. This allows much higher tail currents (and higher slew rates) for a given  $g_m$  when JFETs are used as the input stage.

### ***A New VFB Op Amp Architecture for “Current-on-Demand” Performance, Lower Power, and Improved Slew Rate***

Until recently, op amp designers had to make the above trade-offs between the input  $g_m$  stage quiescent current and the slew rate and distortion performance. ADI has patented a circuit core that supplies *current-on-demand*, to charge and discharge the dominant pole capacitor,  $C_p$ , while allowing the quiescent current to be small. The additional current is proportional to the fast slewing input signal and adds to the quiescent current.

A simplified diagram of the basic core cell is shown in Figure 1-104. The *quad-core* ( $g_m$  stage) consists of transistors Q1, Q2, Q3, and Q4 with their emitters connected together as shown. Consider a positive step voltage on the inverting input. This voltage produces a proportional current in Q1 that is mirrored into  $C_{p1}$  by Q5. The current through Q1 also flows through Q4 and  $C_{p2}$ .

At the dynamic range limit, Q2 and Q3 are correspondingly turned off. Notice that the charging and discharging current for  $C_{p1}$  and  $C_{p2}$  is not limited by the quad core bias current. In practice, however, small current-limiting resistors are required forming an “H” resistor network as shown. Q7 and Q8 form the second gain stage (driven differentially from the collectors of Q5 and Q6), and the output is buffered by a unity-gain complementary emitter follower (X1).



**Figure 1-104: “Quad-Core” VFB  $g_m$  stage for current-on-demand**

The quad core configuration is patented (see Reference 1), as well as the circuits that establish the quiescent bias currents (not shown in Figure 1-104). A number of new VFB op amps using this proprietary configuration have been released and have unsurpassed high frequency low distortion performance, bandwidth, and slew rate at the indicated quiescent current levels as shown in Figure 1-105.

LISTED IN ORDER OF DECREASING SUPPLY CURRENT

PART #	$I_{SY}$ / AMP	BANDWIDTH	SLEWRATE	DISTORTION
AD9631/32 (1)	17mA	320MHz	1300V/ $\mu$ s	-72dBc@20MHz
AD8074/75 (3)	8mA	600MHz	1600V/ $\mu$ s	-62dBc@20MHz
AD8047/48 (1)	5.8mA	250MHz	750V/ $\mu$ s	-66dBc@5MHz
AD8041 (1)	5.2mA	160MHz	160V/ $\mu$ s	-69dBc@10MHz
AD8042 (2)	5.2mA	160MHz	200V/ $\mu$ s	-64dBc@10MHz
AD8044 (3)	2.8mA	150MHz	150V/ $\mu$ s	-75dBc@5MHz
AD8039 (2)	1.5mA	300MHz	425V/ $\mu$ s	-65dBc@5MHz
AD8031 (1)	0.75mA	80MHz	30V/ $\mu$ s	-62dBc@1MHz
AD8032 (2)	0.75mA	80MHz	30V/ $\mu$ s	-72dBc@1MHz

Number in ( ) indicates single, dual, triple, or quad

**Figure 1-105: High speed VFB op amps**

The AD9631, AD8074, and AD8047 are optimized for a gain of +1, while the AD9632, AD8075, and AD8048 for a gain of +2.

The same quad-core architecture is used as the *second* stage of the AD8041 rail-to-rail output, zero-volt input single-supply op amp. The input stage is a differential PNP pair which allows the input common-mode signal to go about 200 mV below the negative supply rail. The AD8042 and AD8044 are dual and quad versions of the AD8041.

## Current Feedback (CFB) Op Amps

We will now examine in more detail the current feedback (CFB) op amp topology which is very popular in high speed op amps. As mentioned previously, the circuit concepts were introduced decades ago; however, modern high speed complementary bipolar processes are required to take full advantage of the architecture.

It has long been known that in bipolar transistor circuits, currents can be switched faster than voltages, other things being equal. This forms the basis of nonsaturating emitter-coupled logic (ECL) and devices such as current-output DACs. Maintaining low impedances at the current switching nodes helps to minimize the effects of stray capacitance, one of the largest detriments to high speed operation. The current mirror is a good example of how currents can be switched with a minimum amount of delay.

The current feedback op amp topology is simply an application of these fundamental principles of current steering. A simplified CFB op amp is shown in Figure 1-106. The noninverting input is high impedance and is buffered directly to the inverting input through the complementary emitter follower buffers Q1 and Q2. Note that the inverting input impedance is very low (typically  $10\ \Omega$  to  $100\ \Omega$ ), because of the low emitter resistance (ideally, would be zero). This is a fundamental difference between a CFB and a VFB op amp, and also a feature that gives the CFB op amp some unique advantages.

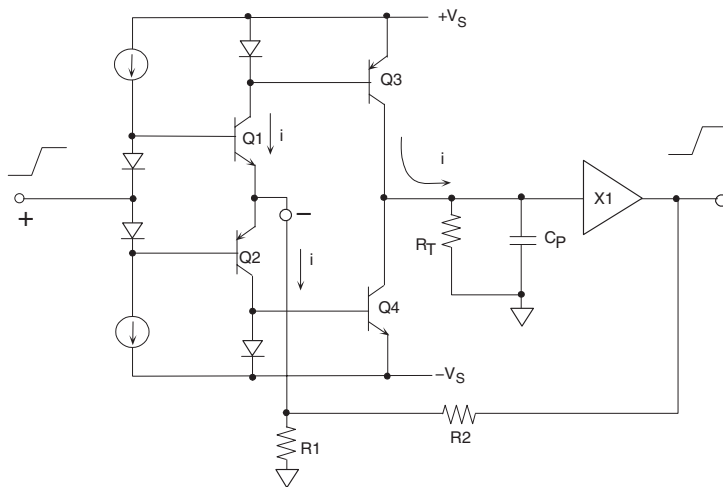


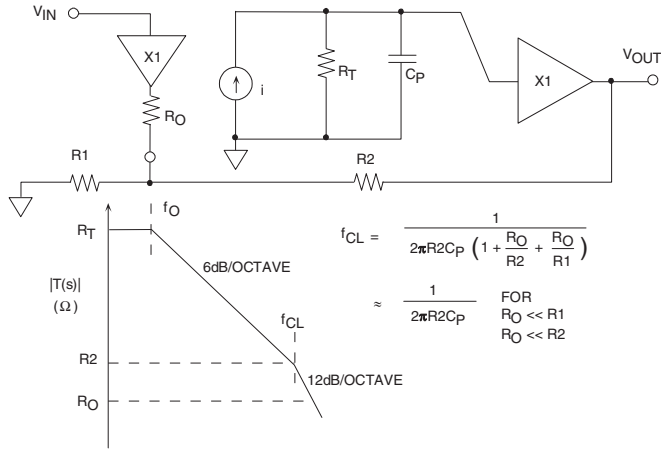
Figure 1-106: Simplified current feedback (CFB) op amp

The collector outputs of Q1 and Q2 drive current mirrors, which mirror the inverting input current to the high impedance node, modeled by  $R_T$  and  $C_P$ . The high impedance node is buffered by a complementary unity gain emitter follower. Feedback from the output to the inverting input acts to force the inverting input *current* to zero, hence the term *Current Feedback*. Note that in an ideal case, for zero inverting input impedance, no small-signal voltage can exist at this node, only small-signal current.

Now, consider a positive step voltage applied to the noninverting input of the CFB op amp. Q1 immediately sources a proportional current into the external feedback resistors creating an *error* current, which is mirrored to the high impedance node by Q3. The voltage developed at the high impedance node is equal to this current multiplied by the equivalent impedance. This is where the term *transimpedance op amp* originated, since the transfer function is an impedance, rather than a unitless voltage ratio as in a traditional VFB op amp.

Note also that the error current delivered to the high impedance node is not limited by the input stage tail current. In other words, unlike a conventional VFB op amp, *there is no slew rate limitation in an ideal CFB op amp*. The current mirrors supply *current-on-demand* from the power supplies. The negative feedback loop then forces the output voltage to a value that reduces the inverting input error current to zero.

The model for a CFB op amp is shown in Figure 1-107, along with the corresponding Bode plot. The Bode plot is plotted on a log-log scale, and the open-loop gain is expressed as a transimpedance,  $T(s)$ , with units of ohms.



**Figure 1-107: CFB op amp model and Bode plot**

The finite output impedance of the input buffer is modeled by  $R_O$ . The input error current is  $i$ . By applying the principles of negative feedback, we can derive the expression for the op amp transfer function:

$$\frac{V_{out}}{V_{in}} = \frac{1 + \frac{R2}{R1}}{1 + j\omega C_p R2 \left( 1 + \frac{R_o}{R2} + \frac{R_o}{R1} \right)} \quad \text{Eq. 1-46}$$

At the op amp 3 dB closed-loop bandwidth frequency,  $f_{cl}$ , the following is true:

$$2\pi f_{cl} C_p R2 \left( 1 + \frac{R_o}{R2} + \frac{R_o}{R1} \right) = 1 \quad \text{Eq. 1-47}$$

$$f_{cl} = \frac{1}{2\pi C_p R2 \left( 1 + \frac{R_o}{R2} + \frac{R_o}{R1} \right)} \quad \text{Eq. 1-48}$$

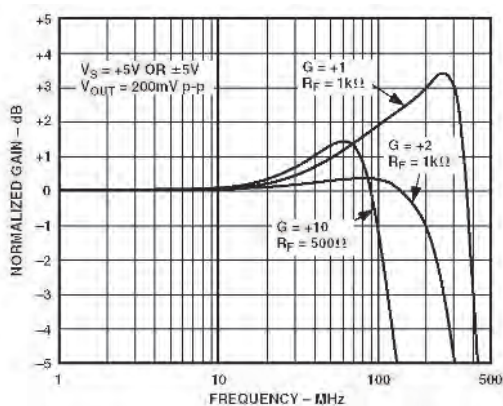
For the condition  $R_o \ll R2$  and  $R1$ , the equation simply reduces to:

$$f_{cl} = \frac{1}{2\pi C_p R2} \quad \text{Eq. 1-49}$$

Examination of this equation quickly reveals that *the closed-loop bandwidth of a CFB op amp is determined by the internal dominant pole capacitor,  $C_p$ , and the external feedback resistor,  $R_2$ , and is independent of the gain-setting resistor,  $R_1$* . This ability to maintain constant bandwidth independent of gain makes CFB op amps ideally suited for wideband programmable gain amplifiers.

Because the closed-loop bandwidth is inversely proportional to the external feedback resistor,  $R_2$ , a CFB op amp is usually optimized for a specific  $R_2$ . Increasing  $R_2$  from its optimum value lowers the bandwidth, and decreasing it may lead to oscillation and instability because of high frequency parasitic poles.

The frequency response of the AD8011 CFB op amp is shown in Figure 1-108 for various closed-loop values of gain (+1, +2, and +10). Note that even at a gain of +10, the closed-loop bandwidth is still greater than 100 MHz. The peaking that occurs at a gain of +1 is typical of wideband CFB op amps used in the noninverting mode, and is due primarily to stray capacitance at the inverting input. This peaking can be reduced by sacrificing bandwidth, by using a slightly larger feedback resistor.



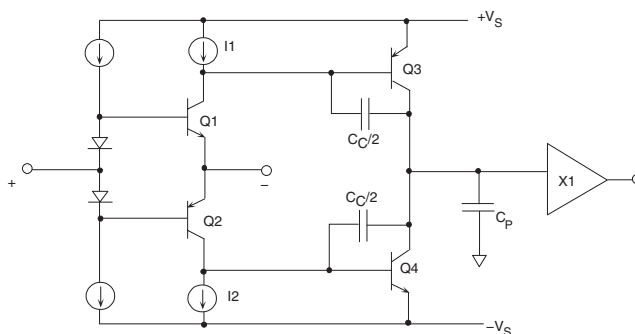
**Figure 1-108: AD8011 frequency response,  $G = +1, +2, +10$**

The AD8011 CFB op amp (introduced in 1995) still represents state-of-the-art performance, and key specifications are shown in Figure 1-109.

- 1mA Power Supply Current (+5V or  $\pm 5V$ )
- 300MHz Bandwidth ( $G = +1$ )
- 2000 V/ $\mu s$  Slew Rate
- 29ns Settling Time to 0.1%
- Video Specifications ( $G = +2$ )
  - Differential Gain Error 0.02%
  - Differential Phase Error 0.06°
  - 25MHz 0.1dB Bandwidth
- Distortion
  - 70dBc @ 5MHz
  - 62dBc @ 20MHz
- Fully Specified for  $\pm 5V$  or +5V Operation

**Figure 1-109: AD8011 key specifications**

Traditional current feedback op amps have been limited to a single gain stage, using current-mirrors. The AD8011 (and also others in this family) unlike traditional CFB op amps, use a *two-stage gain configuration*, as shown in Figure 1-110.



**Figure 1-110: Simplified two-stage current feedback op amp**

Until the advent of the AD8011, fully complementary two-gain stage CFB op amps had been impractical because of their high power dissipation. The AD8011 employs a patented (see Reference 2) second gain stage consisting of a pair of complementary amplifiers (Q3 and Q4). Note that they are not connected as current mirrors but as grounded-emitter gain stages. The detailed design of current sources (I1 and I2), and their respective bias circuits are the key to the success of the two-stage CFB circuit; they keep the amplifier's quiescent power low, yet are capable of supplying *current-on-demand* for wide current excursions required during fast slewing.

A further advantage of the two-stage amplifier is the higher overall bandwidth (for the same power), which means lower signal distortion and the ability to drive heavier external loads.

Thus far, we have learned several key features of CFB op amps. The most important is that for a given complementary bipolar IC process, *CFB generally yields higher FPBW (hence lower distortion) than VFB for the same amount of quiescent supply current*. This is because there is practically no slew-rate limiting in CFB. Because of this, the full power bandwidth and the small signal bandwidth are approximately the same.

The second important feature is that the *inverting input impedance of a CFB op amp is very low*. This is advantageous when using the op amp in the inverting mode as an I/V converter, because there is less sensitivity to inverting input capacitance than with VFB.

The third feature is that *the closed-loop bandwidth of a CFB op amp is determined by the value of the internal C<sub>p</sub> capacitor and the external feedback resistor R<sub>2</sub> and is relatively independent of the gain-setting resistor R<sub>1</sub>*.

The performance for a selected group of current feedback op amps is shown in Figure 1-111. Note that the op amps are listed in order of decreasing power supply current.

LISTED IN ORDER OF DECREASING SUPPLY CURRENT

PART #	$I_{SY}/\text{AMP}$	BANDWIDTH	SLEW RATE	DISTORTION
AD8009 (1)	14mA	1000MHz	5500V/ $\mu\text{s}$	-80dBc@5MHz
AD8023 (3)	10mA	250MHz	1200V/ $\mu\text{s}$	$\Delta G = 0.06\%$ , $\Delta\phi = 0.02^\circ$
AD8001 (1)	5.0mA	600MHz	1200V/ $\mu\text{s}$	-65dBc@5MHz
AD8002 (2)	5.0mA	600MHz	1200V/ $\mu\text{s}$	-65dBc@5MHz
AD8004 (4)	3.5mA	250MHz	3000V/ $\mu\text{s}$	-78dBc@5MHz
AD8013 (3)	4.0mA	140MHz	1000V/ $\mu\text{s}$	$\Delta G = 0.02\%$ , $\Delta\phi = 0.06^\circ$
AD8072 (2)	3.5mA	100MHz	500V/ $\mu\text{s}$	$\Delta G = 0.05\%$ , $\Delta\phi = 0.1^\circ$
AD8073 (3)	3.5mA	100MHz	500V/ $\mu\text{s}$	$\Delta G = 0.05\%$ , $\Delta\phi = 0.1^\circ$
AD8012 (2)	1.7mA	350MHz	2250V/ $\mu\text{s}$	-66dBc@5MHz
AD8014 (1)	1.2mA	400MHz	4000V/ $\mu\text{s}$	-70dBc@5MHz
AD8011 (1)	1.0mA	300MHz	5500V/ $\mu\text{s}$	-70dBc@5MHz
AD8005 (1)	0.4mA	270MHz	1500/ $\mu\text{s}$	-53dBc@5MHz

Number in ( ) Indicates Single, Dual, Triple, or Quad

**Figure 1-111: Performance of selected CFB op amps**

Figure 1-112 summarizes the general characteristics of CFB op amps.

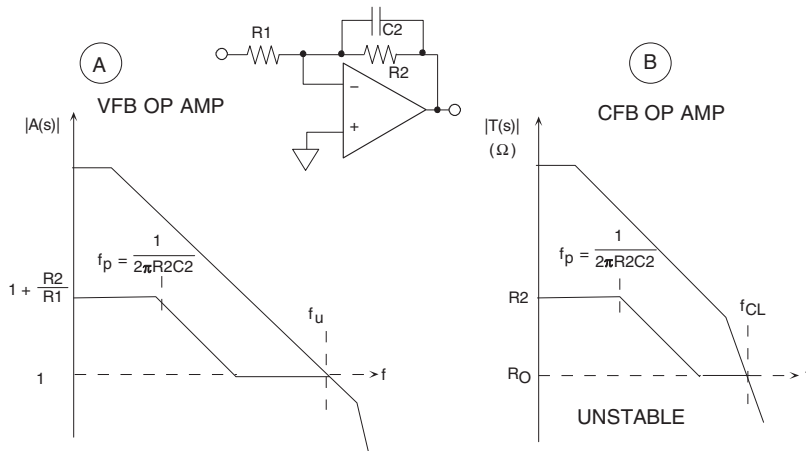
- CFB yields higher FPBW and lower distortion than VFB for the same process and power dissipation
- Inverting input impedance of a CFB op amp is low, noninverting input impedance is high
- Closed-loop bandwidth of a CFB op amp is determined by the internal dominant-pole capacitance and the external feedback resistor, independent of the gain-setting resistor

**Figure 1-112: Summary: CFB op amps**

## Effects of Feedback Capacitance in Op Amps

It is quite common to use a capacitor in the feedback loop of a VFB op amp, to shape the frequency response as in a simple single-pole lowpass filter shown in Figure 1-113A. The resulting noise gain is plotted on a Bode plot to analyze stability and phase margin. Stability of the system is determined by the net slope of the noise gain and the open-loop gain where they intersect.

For unconditional stability, the noise gain plot must intersect the open-loop response with a net slope of less than 12 dB/octave. In this case, the net slope where they intersect is 6 dB/octave, indicating a stable condition. Notice for the case drawn in Figure 1-113A, the second pole in the frequency response occurs at a considerably higher frequency than  $f_u$ .

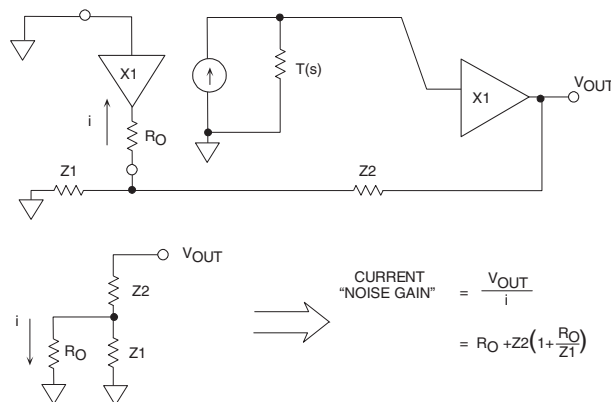


**Figure 1-113: Noise gain stability analysis for VFB and CFB op amps with feedback capacitor**

In the case of the CFB op amp (Figure 1-113B), the same analysis is used, except that the open-loop transimpedance gain,  $T(s)$ , is used to construct the Bode plot.

The definition of *noise gain* (for the purposes of stability analysis) for a CFB op amp, however, must be redefined in terms of a *current* noise source attached to the inverting input as shown in Figure 1-114. This current is reflected to the output by an impedance, which we define to be the “current noise gain” of a CFB op amp:

$$\text{“CURRENT NOISE GAIN”} \equiv R_o + Z_2 \left( 1 + \frac{R_o}{Z_1} \right) \quad \text{Eq. 1-50}$$



**Figure 1-114: Current “noise gain” definition for CFB op amp for use in stability analysis**



Now, return to Figure 1-113B, and observe the CFB *current noise gain* plot. At low frequencies, the CFB current noise gain is simply  $R_2$  (making the assumption that  $R_o$  is much less than  $Z_1$  or  $Z_2$ ). The first pole is determined by  $R_2$  and  $C_2$ . As the frequency continues to increase,  $C_2$  becomes a short circuit, and all the inverting input current flows through  $R_o$  (again refer to Figure 1-114).

A CFB op amp is normally optimized for best performance for a fixed feedback resistor,  $R_2$ . Additional poles in the transimpedance gain,  $T(s)$ , occur at frequencies above the closed-loop bandwidth,  $f_{cl}$ , (set by  $R_2$ ). Note that the intersection of the CFB current noise gain with the open-loop  $T(s)$  occurs where the slope of the  $T(s)$  function is 12 dB/octave. This indicates instability and possible oscillation.

It is for this reason that *CFB op amps are not suitable in configurations that require capacitance in the feedback loop*, such as simple active integrators or low-pass filters.

They can, however, be used in certain active filters, such as the Sallen-Key configuration shown in Figure 1-115, which do not require capacitance in the feedback network.

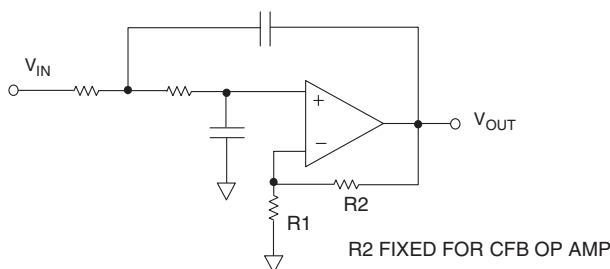


Figure 1-115: The Sallen-Key filter configuration

On the other hand, VFB op amps do make very flexible active filters. A multiple feedback 20 MHz low-pass filter example using an AD8048 op amp is shown in Figure 1-116.

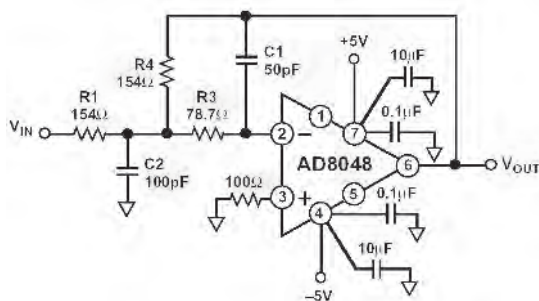


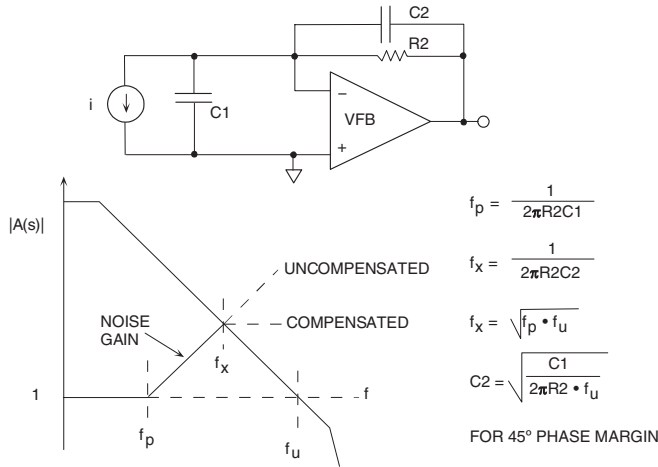
Figure 1-116: Multiple feedback 20 MHz low-pass filter using the AD8048 VFB op amp

In general, an active filter amplifier should have a bandwidth that is at least 10 times the bandwidth of the filter, if problems due to phase shift of the amplifier are to be avoided. (The AD8048 has a bandwidth of over 200 MHz in this configuration.)

Design details of the filter design can be found on the AD8048 data sheet. Further discussions on active filter design are included in Chapter 5 of this book.

## High Speed Current-to-Voltage Converters, and the Effects of Inverting Input Capacitance

Fast op amps are useful as current-to-voltage converters in such applications as high speed photodiode pre-amplifiers and current-output DAC buffers. A typical application using a VFB op amp as an I/V converter is shown in Figure 1-117.



**Figure 1-117: Compensating for input capacitance in a current-to-voltage converter using VFB op amp**

The net input capacitance,  $C1$ , forms a pole at a frequency  $f_p$  in the noise gain transfer function as shown in the Bode plot, and is given by:

$$f_p = \frac{1}{2\pi R2 C1} \quad \text{Eq. 1-51}$$

If left uncompensated, the phase shift at the frequency of intersection,  $f_x$ , will cause instability and oscillation. Introducing a zero at  $f_x$  by adding feedback capacitor  $C2$  stabilizes the circuit and yields a phase margin of about 45°.

The location of the zero is given by:

$$f_x = \frac{1}{2\pi R2 C2} \quad \text{Eq. 1-52}$$

Although the addition of  $C2$  actually decreases the pole frequency slightly, this effect is negligible if  $C2 \ll C1$ . The frequency  $f_x$  is the geometric mean of  $f_p$  and the unity-gain bandwidth frequency of the op amp,  $f_u$ ,

$$f_x = \sqrt{f_p \cdot f_u} \quad \text{Eq. 1-53}$$

Combining Eq. 1-52 and Eq. 1-53 and solving for  $C2$  yields:

$$C2 = \sqrt{\frac{C1}{2\pi R2 \cdot f_u}} \quad \text{Eq. 1-54}$$

This value of  $C_2$  will yield a phase margin of about  $45^\circ$ . Increasing the capacitor by a factor of 2 increases the phase margin to about  $65^\circ$  (see Reference 3).

In practice, the optimum value of  $C_2$  may be optimized experimentally by varying it slightly, to optimize the output pulse response.

A similar analysis can be applied to a CFB op amp as shown in Figure 1-118. In this case, however, the low inverting input impedance,  $R_O$ , greatly reduces the sensitivity to input capacitance. In fact, an ideal CFB with zero input impedance would be totally insensitive to any amount of input capacitance.

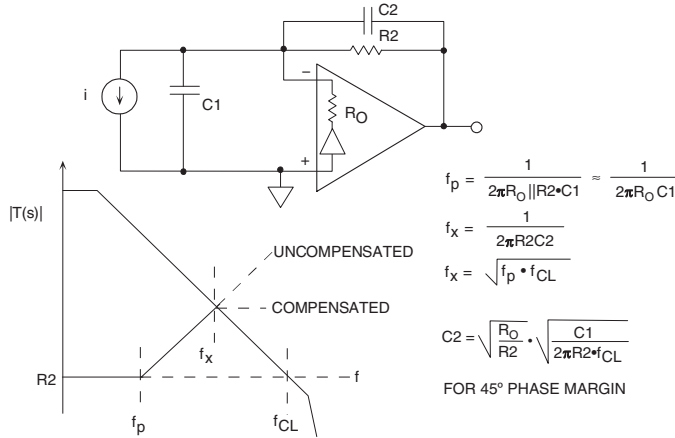


Figure 1-118: Current-to-voltage converter using a CFB op amp

The pole caused by  $C_1$  occurs at a frequency  $f_p$ :

$$f_p = \frac{1}{2\pi (R_O \parallel R_2) C_1} \approx \frac{1}{2\pi R_O C_1} \quad \text{Eq. 1-55}$$

This pole frequency will generally be much higher than the case for a VFB op amp, and the pole can be ignored completely if it occurs at a frequency greater than the closed-loop bandwidth of the op amp.

We next introduce a compensating zero at the frequency  $f_x$  by inserting the capacitor  $C_2$ :

$$f_x = \frac{1}{2\pi R_2 C_2} \quad \text{Eq. 1-56}$$

As in the case for VFB,  $f_x$  is the geometric mean of  $f_p$  and  $f_{cl}$ :

$$f_x = \sqrt{f_p \cdot f_{cl}} \quad \text{Eq. 1-57}$$

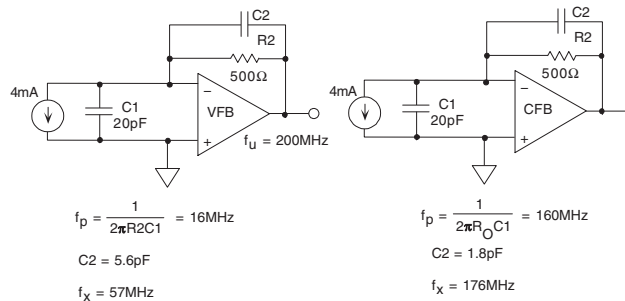
Combining Eq. 1-56 and Eq. 1-57 and solving for  $C_2$  yields:

$$C_2 = \sqrt{\frac{R_O}{R_2}} \cdot \sqrt{\frac{C_1}{2\pi R_2 \cdot f_{cl}}} \quad \text{Eq. 1-58}$$

There is a significant advantage in using a CFB op amp in this configuration as can be seen by comparing Eq. 1-58 with the similar equation for  $C_2$  required for a VFB op amp, Eq. 1-54. If the unity-gain bandwidth

product of the VFB is equal to the closed-loop bandwidth of the CFB (at the optimum  $R_2$ ), then the size of the CFB compensation capacitor,  $C_2$ , is reduced by a factor of  $\sqrt{(R_2/R_o)}$ .

A comparison in an actual application is shown in Figure 1-119. The full scale output current of the DAC is 4 mA, the net capacitance at the inverting input of the op amp is 20 pF, and the feedback resistor is 500  $\Omega$ . In the case of the VFB op amp, the pole due to  $C_1$  occurs at 16 MHz. A compensating capacitor of 5.6 pF is required for 45° of phase margin, and the signal bandwidth is 57 MHz.

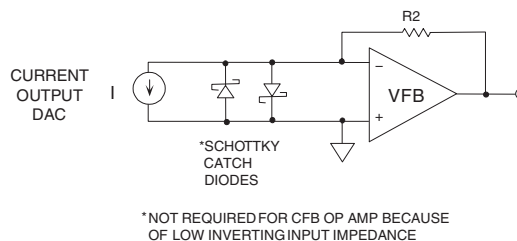


**Figure 1-119: CFB op amp is relatively insensitive to input capacitance when used as an I/V converter**

For the CFB op amp, however, because of the low inverting input impedance ( $R_o = 50\Omega$ ), the pole occurs at 160 MHz, the required compensation capacitor is about 1.8 pF, and the corresponding signal bandwidth is 176 MHz. In practice, the pole frequency is so close to the closed-loop bandwidth of the op amp that it could probably be left uncompensated.

It should be noted that a CFB op amp's relative insensitivity to inverting input capacitance is when it is used in the inverting mode. In the noninverting mode, however, even a few picofarads of stray capacitance on the inverting input can cause significant gain peaking and potential instability.

Another advantage of the low inverting input impedance of the CFB op amp is when it is used as an I/V converter to buffer the output of a high speed current output DAC. When a step function current (or DAC switching glitch) is applied to the inverting input of a VFB op amp, it can produce a large voltage transient until the signal can propagate through the op amp to its output and negative feedback is regained. Back-to-back Schottky diodes are often used to limit this voltage swing as shown in Figure 1-120. These diodes must be low capacitance, small geometry devices because their capacitance adds to the total input capacitance.



**Figure 1-120: Low inverting input impedance of CFB op amp helps reduce effects of fast DAC transients**

A CFB op amp, on the other hand, presents a low impedance ( $R_o$ ) to fast switching currents even before the feedback loop is closed, thereby limiting the voltage excursion without the requirement of the external diodes. This greatly improves the settling time of the I/V converter.

### **Noise Comparisons between VFB and CFB Op Amps**

In most applications of high speed op amps, it is generally the total output RMS noise that is of interest. Because of the high bandwidths involved, the chief contributor to the output RMS noise is therefore the white noise, and the  $1/f$  noise is negligible.

Typical high speed op amps with bandwidths greater than 150 MHz or so, and bipolar VFB input stages, have input voltage noises ranging from about 2 nV to 20 nV/ $\sqrt{\text{Hz}}$ .

For a VFB op amp, the inverting and noninverting input current noise are typically equal, and almost always uncorrelated. Typical values for wideband VFB op amps range from 0.5 pA/ $\sqrt{\text{Hz}}$  to 5 pA/ $\sqrt{\text{Hz}}$ . The input current noise of a bipolar input stage is increased when input bias-current compensation generators are added, because their current noise is not correlated, and therefore adds (in an RSS manner) to the intrinsic current noise of the bipolar stage. However, bias current compensation is rarely used in high speed op amps.

The input voltage noise in CFB op amps tends to be lower than for VFB op amps having the same approximate bandwidth. This is because the input stage in a CFB op amp is usually operated at a higher current, thereby reducing the emitter resistance and hence the voltage noise. Typical values for CFB op amps range from about 1 nV to 5 nV/ $\sqrt{\text{Hz}}$ .

The input current noise of CFB op amps tends to be larger than for VFB op amps because of the generally higher bias current levels. The inverting and noninverting current noise of a CFB op amp is usually different because of the unique input architecture, and are specified separately. In most cases, the inverting input current noise is the larger of the two. Typical input current noise for CFB op amps ranges from 5 pA to 40 pA/ $\sqrt{\text{Hz}}$ . This can often be dominant, except in cases of very high gain, when  $R_1$  is small.

The noise sources that dominate the output noise are highly dependent on the closed-loop gain of the op amp and the values of the feedback and feedforward resistors. For high values of closed-loop gain, the op amp voltage noise will tend to be the chief contributor to the output noise. At low gains, the effects of the input current noise must also be considered, and may dominate, especially in the case of a CFB op amp.

Feedforward/feedback resistors in high speed op amp circuits may range from less than 100  $\Omega$  to more than 1 k $\Omega$ , so it is difficult to generalize about their contribution to the total output noise without knowing the specific values and the closed-loop gain.

The best way to make the noise calculations is to write a simple computer program that automatically performs the calculations, and include all the noise sources. The equation previously discussed can be used for this purpose (see Figure 1-74). In most high speed op amp applications, the source impedance noise can often be neglected for source impedances of 100  $\Omega$  or less.

Figure 1-121 summarizes the noise characteristics of high speed op amps.

- Voltage Feedback Op Amps:
  - Voltage noise: 2nV to 20nV/ $\sqrt{\text{Hz}}$
  - Current noise: 0.5pA to 5pA/ $\sqrt{\text{Hz}}$
- Current Feedback Op Amps:
  - Voltage noise: 1nV to 5nV/ $\sqrt{\text{Hz}}$
  - Current noise: 5nV to 40pA/ $\sqrt{\text{Hz}}$
- Noise Contribution from Source Negligible if  $< 100\Omega$
- Voltage Noise Usually Dominates at High Gains
- Reflect Noise Sources to Output and Combine (RSS)
- Errors Will Result if there is Significant High Frequency Peaking

**Figure 1-121: High speed op amp noise summary**

## ***DC Characteristics of High Speed Op Amps***

High speed op amps are optimized for bandwidth and settling time, not for precision dc characteristics as found in lower frequency precision op amps. In spite of this, however, high speed op amps do have reasonably good dc performance.

Input offset voltages of high speed bipolar input op amps are rarely trimmed, since offset voltage matching of the input stage is excellent, typically ranging from 1 mV to 3 mV, with offset temperature coefficients of 5  $\mu\text{V}$  to 15  $\mu\text{V}/^\circ\text{C}$ .

Input bias currents on VFB op amps (with no input bias current compensation circuits) are approximately equal for (+) and (–) inputs, and can range from 1  $\mu\text{A}$  to 5  $\mu\text{A}$ . The output offset voltage due to the input bias currents can be nulled by making the effective source resistance,  $R_3$ , equal to the parallel combination of  $R_1$  and  $R_2$ .

As previously discussed, this scheme will not work with bias-current compensated VFB op amps that have additional current generators on their inputs. In this case, the net input bias currents are not necessarily equal or of the same polarity.

CFB op amps generally have unequal and uncorrelated input bias currents because the (+) and (–) inputs have completely different architectures. For this reason, external bias current cancellation schemes are also ineffective. CFB input bias currents range from 5  $\mu\text{A}$  to 15  $\mu\text{A}$ , being generally higher at the inverting input.

Figure 1-122 summarizes the offset considerations for high speed op amps.

- High Speed Bipolar Op Amp Input Offset Voltage:
  - Ranges from 1mV to 3mV for VFB and CFB
  - Offset TC ranges from 5 $\mu$ V to 15 $\mu$ V/ $^{\circ}$ C
- High Speed Bipolar Op Amp Input Bias Current:
  - For VFB ranges from 1 $\mu$ A to 5 $\mu$ A
  - For CFB ranges from 5 $\mu$ A to 15 $\mu$ A
- Bias Current Cancellation Doesn't Work for:
  - Bias current compensated op amps
  - Current feedback op amps

**Figure 1-122: High speed op amp offset voltage summary**

## References: High Speed Op Amps

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7. Data sheet for **AD8011 300 MHz, 1 mA Current Feedback Amplifier**, [www.analog.com](http://www.analog.com).

## CHAPTER 2

# *Specialty Amplifiers*

- Section 2-1: Instrumentation Amplifiers
- Section 2-2: Programmable Gain Amplifiers
- Section 2-3: Isolation Amplifiers



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# *Specialty Amplifiers*

*Walt Kester, Walt Jung, James Bryant*

This chapter of the book discusses several popular types of *specialty* amplifiers, or amplifiers that are based in some way on op amp techniques. However, in an overall applications sense, they are not generally used as universally as op amps. Examples of specialty amplifiers include instrumentation amplifiers of various configurations, programmable gain amplifiers (PGAs), isolation amplifiers, and difference amplifiers.

Other types of amplifiers, for example such types as audio and video amplifiers, cable drivers, high-speed variable gain amplifiers (VGAs), and various communications-related amplifiers might also be viewed as specialty amplifiers. However, these applications are more suitably covered in Chapter 6, within the various signal amplification sections.

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# Instrumentation Amplifiers

Walt Kester, Walt Jung

Probably the most popular among all of the specialty amplifiers is the *instrumentation amplifier* (hereafter called simply an *in amp*). The in amp is widely used in many industrial and measurement applications where dc precision and gain accuracy must be maintained within a noisy environment, and where large common-mode signals (usually at the ac power line frequency) are present.

## Op Amp/In Amp Functionality Differences

An in amp is unlike an op amp in a number of very important ways. As already discussed, an op amp is a general-purpose gain block—user-configurable in myriad ways using external feedback components of R, C, and, (sometimes) L. The final configuration and circuit function using an op amp is truly whatever the user makes of it.

In contrast to this, an in amp is a more constrained device in terms of functioning, and also the allowable range(s) of operating gain. In many ways, it is better suited to its task than would be an op amp—even though, ironically, an in amp may actually comprise of a number of op amps within it. People also often confuse in amps as to their function, calling them “op amps.” But the reverse is seldom (if ever) true. It should be understood that an in amp is *not* just a special type op amp; the function of the two devices is fundamentally different.

Perhaps a good way to differentiate the two devices is to remember that an op amp can be programmed to do almost anything, by virtue of its feedback flexibility. In contrast to this, an in amp *cannot* be programmed to do just anything. It can *only* be programmed for gain, and then over a specific range. An op amp is configured via a number of external components, while an in amp is configured either by one resistor, or by pin-selectable taps for its working gain.

## In Amp Definitions

An in amp is a *precision* closed-loop gain block. It has a pair of differential input terminals, and a single-ended output that works with respect to a reference or common terminal, as shown in Figure 2-1. The input impedances are balanced and high in value, typically  $\geq 10^9 \Omega$ . Again, unlike an op amp, an in amp uses an

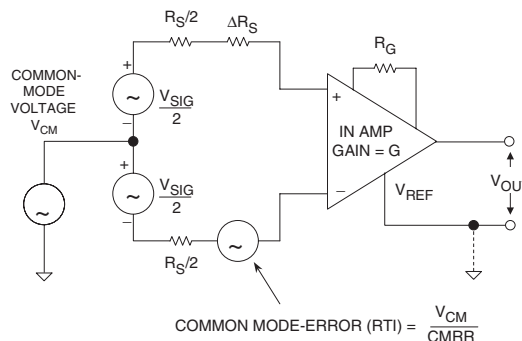


Figure 2-1: The generic instrumentation amplifier (in amp)

internal feedback resistor network, plus one (usually) gain set resistance,  $R_G$ . Also unlike an op amp is the fact that the internal resistance network and  $R_G$  are *isolated* from the signal input terminals. In amp gain can also be preset via an internal  $R_G$  by pin selection, (again isolated from the signal inputs). Typical in amp gains range from 1 to 1,000.

The in amp develops an output voltage that is referenced to a pin usually designated REFERENCE, or  $V_{REF}$ . In many applications, this pin is connected to circuit ground, but it can be connected to other voltages, as long as they lie within a rated compliance range. This feature is especially useful in single-supply applications, where the output voltage is usually referenced to mid-supply (i.e., 2.5 V in the case of a +5 V supply).

In order to be effective, an in amp needs to be able to amplify microvolt-level signals, while simultaneously rejecting volts of *common-mode* (CM) signal at its inputs. This requires that in amps have very high *common-mode rejection* (CMR). Typical values of in amp CMR are from 70 dB to over 100 dB, with CMR usually improving at higher gains.

It is important to note that a CMR specification for dc inputs alone isn't sufficient in most practical applications. In industrial applications, the most common cause of external interference is 50 Hz/60 Hz ac power-related noise (including harmonics). In differential measurements, this type of interference tends to be induced equally onto both in amp inputs, so the interference appears as a CM input signal. Therefore, specifying CMR over frequency is just as important as specifying its dc value. Note that imbalance in the two source impedances can degrade the CMR of some in amps. Analog Devices fully specifies in amp CMR at 50 Hz/60 Hz, with a source impedance imbalance of 1 k $\Omega$ .

## Subtractor or Difference Amplifiers

A simple subtractor or difference amplifier can be constructed with four resistors and an op amp, as shown in Figure 2-2. It should be noted that this is *not* a true in amp (based on the previously discussed criteria), but it is often used in applications where a simple differential-to-single-ended conversion is required. Because of its popularity, this circuit will be examined in more detail, in order to understand its fundamental limitations before discussing true in amp architectures.

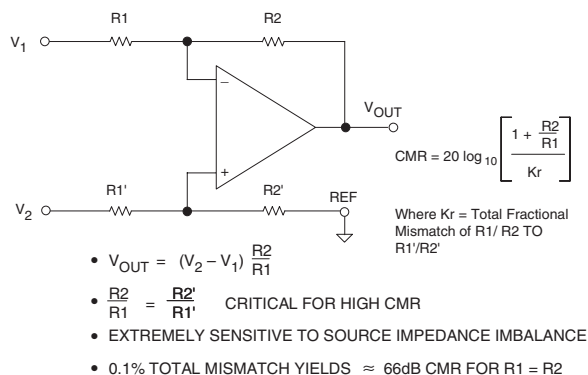


Figure 2-2: Op amp subtractor or difference amplifier

There are several fundamental problems with this simple circuit. First, the input impedance seen by  $V_1$  and  $V_2$  isn't balanced. The input impedance seen by  $V_1$  is  $R_1$ , but the input impedance seen by  $V_2$  is  $R_1' + R_2'$ . The configuration can also be quite problematic in terms of CMR, since even a small source impedance imbalance will degrade the workable CMR. This problem can be solved with well-matched open-loop

buffers in series with each input (for example, using a precision dual op amp). But, this adds complexity to a simple circuit, and may introduce offset drift and nonlinearity.

The second problem with this circuit is that the *CMR is primarily determined by the resistor ratio matching, not the op amp*. The resistor ratios  $R1/R2$  and  $R1'/R2'$  must match extremely well to reject common mode noise—at least as well as a typical op amp CMR of  $\geq 100$  dB. Note also that the *absolute* resistor values are relatively unimportant.

Picking four 1% resistors from a single batch may yield a net ratio matching of 0.1%, which will achieve a CMR of 66 dB (assuming  $R1 = R2$ ). But if one resistor differs from the rest by 1%, the CMR will drop to only 46 dB. Clearly, very limited performance is possible using ordinary discrete resistors in this circuit (without resorting to hand matching). This is because the best standard off-the-shelf RNC/RNR style resistor tolerances are on the order of 0.1% (see Reference 1).

In general, the worst-case CMR for a circuit of this type is given by the following equation (see References 2 and 3):

$$\text{CMR (dB)} = 20 \log \left[ \frac{1 + R2/R1}{4Kr} \right], \quad \text{Eq. 2-1}$$

where  $Kr$  is the *individual* resistor tolerance in fractional form, for the case where four discrete resistors are used. This equation shows that the worst-case CMR for a tolerance build-up for four unselected same-nominal-value 1% resistors to be no better than 34 dB.

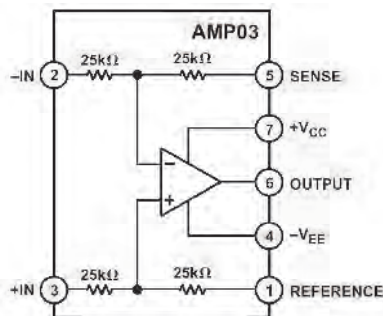
A single resistor network with a net matching tolerance of  $Kr$  would probably be used for this circuit, in which case the expression would be as noted in the figure, or:

$$\text{CMR (dB)} = 20 \log \left[ \frac{1 + R2/R1}{Kr} \right] \quad \text{Eq. 2-2}$$

A net matching tolerance of 0.1% in the resistor ratios therefore yields a worst-case dc CMR of 66 dB using Eq. 2-2, and assuming  $R1 = R2$ . Note that either case assumes a significantly higher amplifier CMR (i.e.,  $>100$  dB). Clearly for high CMR, such circuits need four single-substrate resistors, with very high absolute and TC matching. Such networks using thick/thin-film technology are available from companies such as Caddock and Vishay, in ratio matches of 0.01% or better.

In implementing the simple difference amplifier, rather than incurring the higher costs and PCB real estate limitations of a precision op amp plus a separate resistor network, it is usually better to seek out a completely monolithic solution. The AMP03 is just such a precision difference amplifier, which includes an on-chip laser trimmed precision thin film resistor network. It is shown in Figure 2-3. The typical CMR of the AMP03F is 100 dB, and the small-signal bandwidth is 3 MHz.

**Figure 2-3: AMP03 precision difference amplifier**



There are several devices related to the AMP03 in function. These are namely the SSM2141 and SSM2143 difference amplifiers. These sister parts are designed for audio line receivers (see Figure 2-4). They have low distortion, and high (pretrimmed) CMR. The net gains of the SSM2141 and SSM2143 are unity and 0.5, respectively. They are designed to be used with balanced 600  $\Omega$  audio sources (see the related discussions on these devices in the Audio Amplifiers section of Chapter 6).

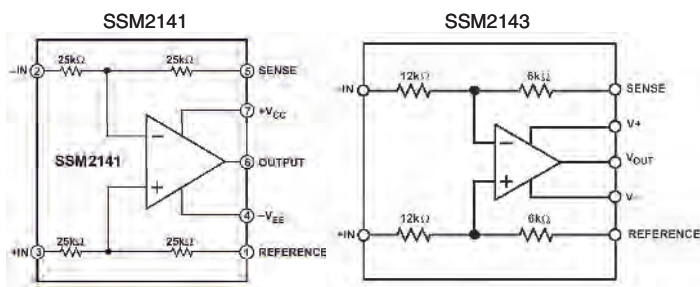


Figure 2-4: SSM2141 and SSM2143 difference amplifiers (audio line receivers)

Another interesting variation on the simple difference amplifier is found in the AD629 difference amplifier, optimized for high common-mode input voltages. A typical current-sensing application is shown in Figure 2-5. The AD629 is a differential-to-single-ended amplifier with a gain of unity. It can handle a common-mode voltage of  $\pm 270$  V with supply voltages of  $\pm 15$  V, with a small signal bandwidth of 500 kHz.

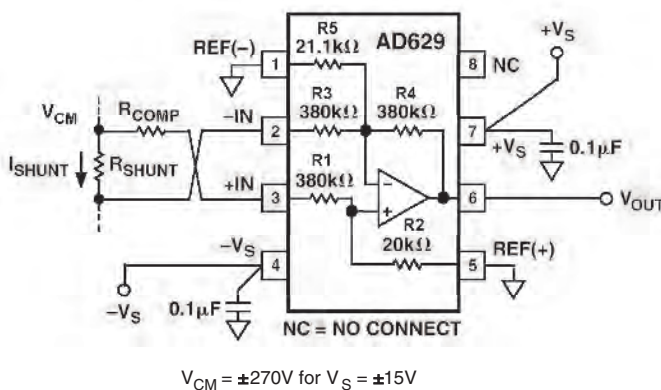
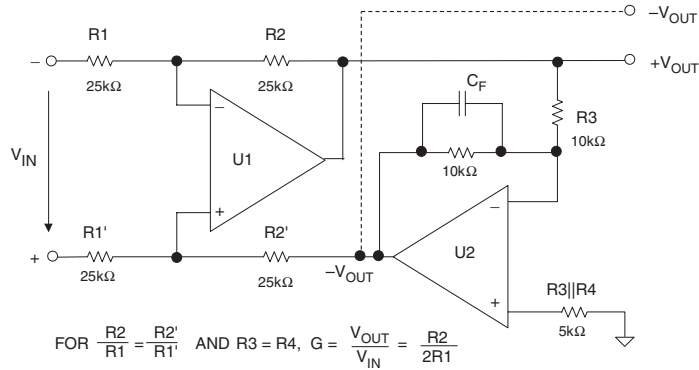


Figure 2-5: High common-mode current sensing using the AD629 difference amplifier

The high common-mode voltage range is obtained by attenuating the noninverting input (Pin 3) by a factor of 20 times, using the R1–R2 divider network. On the inverting input, resistor R5 is chosen such that  $R5 \parallel R3$  equals resistor R2. The noise gain of the circuit is equal to  $20 [1 + R4/(R3 \parallel R5)]$ , thereby providing unity gain for differential input voltages. Laser wafer trimming of the R1–R5 thin film resistors yields a minimum CMR of 86 dB @ 500 Hz for the AD629B. Within an application, it is good practice to maintain

balanced source impedances on both inputs, so dummy resistor  $R_{\text{COMP}}$  is chosen to equal to the value of the shunt sensing resistor  $R_{\text{SHUNT}}$ .

David Birt (see Reference 4) of the BBC has analyzed the simple line receiver topology in terms of loading presented to the source, and presented a modified and balanced form, shown as Figure 2-6. Here stage U1 uses a 4 resistor network identical to that of Figure 2-2, while feedback from the added unity gain inverter U2 drives the previously grounded  $R2'$  reference terminal. This has two overall effects; the input currents in the  $\pm$  input legs become equal in magnitude, and the gain of the stage is halved.



**Figure 2-6: Balanced difference amplifier using push-pull feedback path**

Compared to Figure 2-2, and for like resistor ratios, the Figure 2-6 gain from  $V_{\text{IN}}$  to  $V_{\text{OUT}}$  is one-half, or a gain of  $-6$  dB (0.5) as shown. However the new circuit form also offers a complementary output from U2,  $-V_{\text{OUT}}$ .

The common-mode range of this circuit is the same as for Figure 2-2, but the CMR is about doubled with all resistors nominally equal (as measured to a single output). The inverter resistor ratio  $R3/R4$  affects output balance, but not CMR. Like Figure 2-2, the gain of this circuit is not easily changed, as it involves precise resistor ratios.

Because of the two feedback paths, this circuit holds the inputs of U1 at a null for differential input signals. However CM signals are seen by U1, and the CM range of the circuit is  $[1 + (R2'/R1')] \times V_{\text{CM}(U1)}$ . Differential input resistance is  $R1 + R1'$ .

As can be noted from Figure 2-6, this circuit can be broken into a simple line receiver (left), plus an inverter (right). Thus existing line receivers like Figure 2-2 can be converted to the fully balanced topology, by simply adding an appropriate inverter, U2. This of course not only balances the *input* currents, but it also provides a balanced *output* signal.

For example, the SSM2141 line receiver and the OP275 are a good combination for implementing this approach. (See Reference 5, and the further discussions on these circuits in the Audio Amplifiers section of Chapter 6.)



## Two-Op-Amp In Amps

$$G = 1 + \frac{R_2}{R_1} + \frac{2R_2}{R_G}$$

$$V_{OUT} = (V_2 - V_1) \left[ 1 + \frac{R_2}{R_1} + \frac{2R_2}{R_G} \right] + V_{REF}$$

$$\frac{R_2}{R_1} = \frac{R_2'}{R_1'}$$

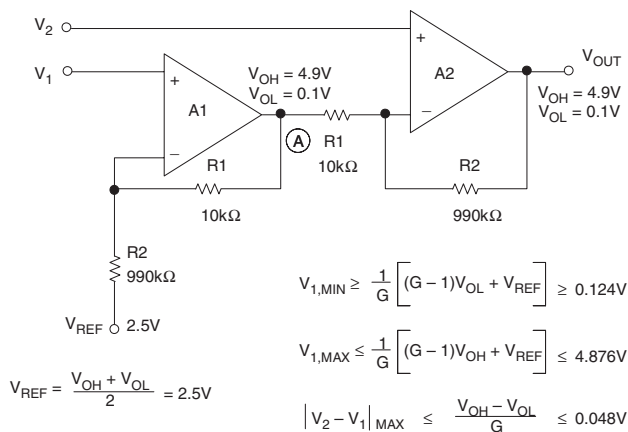
$$CMR \leq 20 \log \left[ \frac{GAIN \times 100}{\% \text{ MISMATCH}} \right]$$

$$\text{CMR} \leq 20 \log \left[ \frac{\text{GAIN} \times 100}{\% \text{MISMATCH}} \right]. \quad \text{Eq. 2-3}$$

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Using the Figure 2-8 equations, the voltage at  $V_1$  must fall between 1.3 V and 2.4 V to prevent A1 from saturating. Notice that  $V_{REF}$  is connected to the average of  $V_{OH}$  and  $V_{OL}$  (2.5 V). This allows for bipolar differential input signals with  $V_{OUT}$  referenced to 2.5 V. A high gain ( $G = 100$ ) single-supply two-op-amp in amp configuration is shown in Figure 2-9. Using the same equations, note that voltage at  $V_1$  can now swing between 0.124 V and 4.876 V.  $V_{REF}$  is again 2.5 V, to allow for bipolar input and output signals.



**Figure 2-9: Two-op-amp in amp single-supply restrictions for  $V_s = +5$  V,  $G = 100$**

All of these discussions show that the conventional two-op-amp in amp architecture is fundamentally limited, when operating from a single power supply. These limitations can be viewed in one sense as a restraint on the allowable input CM range for a given gain. Or, alternately, it can be viewed as limitation on the allowable gain range, for a given CM input voltage.

Nevertheless, there are ample cases where a combination of gain and CM voltage cannot be supported by the basic two-op-amp structures of Figures 2-7 through 2-9, even with perfect amplifiers (i.e., zero output saturation voltage to both rails).

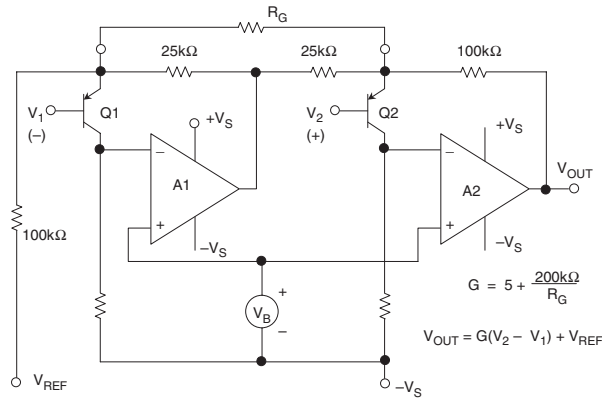
In summary, regardless of gain, the basic structure of the common two-op-amp in amp does not allow for CM input voltages of zero when operated on a single supply. The only route to removing these restrictions for single supply operation is to modify the in amp architecture.

## The AD627 Single-Supply Two-Op-Amp In Amp

The above-mentioned CM limitations can be overcome with some key modifications to the basic two-op-amp in amp architecture. These modifications are implemented in the circuit shown in Figure 2-10, which represents the AD627 in amp architecture.

In this circuit, each of the two op amps is composed of a PNP common emitter input stage and a gain stage, designated Q1/A1, and Q2/A2, respectively. The PNP transistors not only provide gain but also level-shift the input signal positive by about 0.5 V, thereby allowing the common-mode input voltage to go to 0.1 V below the negative supply rail. The maximum positive input voltage allowed is 1 V less than the positive supply rail.

The AD627 in amp delivers rail-to-rail output swing, and operates over a wide supply voltage range (+2.7 V to  $\pm 18$  V). Without the external gain setting resistor  $R_G$ , the in amp gain is a minimum of 5. Gains



**Figure 2-10: The AD627 in amp architecture**

up to 1000 can be set with the addition of this external resistor. Common-mode rejection of the AD627B at 60 Hz with a 1 kΩ source imbalance is 85 dB when operating on a single 3 V supply and  $G = 5$ .

Even though the AD627 is a two-op-amp in amp, it is worthwhile noting that it is not subject to the same CM frequency response limitations as the basic circuit of Figure 2-7. A patented circuit keeps the AD627 CMR flat out to a much higher frequency than would otherwise be achievable with a conventional discrete two-op-amp in amp.

The AD627 data sheet has a detailed discussion of allowable input/output voltage ranges as a function of gain and power supply voltages (see Reference 7). In addition, interactive design tools that perform calculations relating these parameters for a number of in amps, including the AD627 are available on the ADI Web site.

Key specifications for the AD627 are summarized in Figure 2-11. Although it has been designed as a low power, single-supply device, the AD627 is capable of operating on traditional higher voltage supplies such as  $\pm 15$  V, with excellent performance.

- Wide Supply Range: +2.7V to  $\pm 18$ V
- Input Voltage Range:  $-V_S - 0.1$ V to  $+V_S - 1$ V
- 85μA Supply Current
- Gain Range: 5 to 1000
- 75μV Maximum Input Offset Voltage (AD627B)
- 10ppm/°C Maximum Offset Voltage TC (AD627B)
- 10ppm Gain Nonlinearity
- 85dB CMR @ 60Hz, 1kΩ Source Imbalance ( $G = 5$ )
- 3μV p-p 0.1Hz to 10Hz Input Voltage Noise ( $G = 5$ )

**Figure 2-11: AD627 in amp key specifications**

### Three-Op-Amp In Amps

A second popular in amp architecture is based on three op amps, and is shown in Figure 2-12. This circuit is typically referred to as the *three-op-amp in amp*.

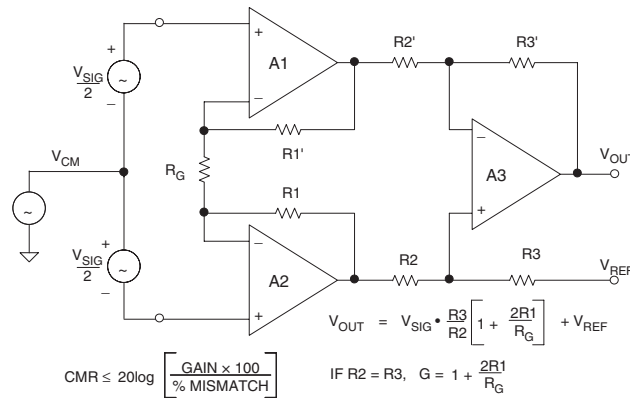


Figure 2-12: The three-op-amp in amp

Resistor  $R_G$  sets the overall gain of this amplifier. It may be internal, external, or (software or pin-strap) programmable, depending upon the in amp. In this configuration, CMR depends upon the ratio-matching of  $R3/R2$  to  $R3'/R2'$ . Furthermore, common-mode signals are only amplified by a factor of 1, regardless of gain. (No common-mode voltage will appear across  $R_G$ , hence, no common-mode current will flow in it because the input terminals of an op amp will have no significant potential difference between them.)

As a result of the high ratio of differential-to-CM gain in A1–A2, CMR of this in amp theoretically increases in proportion to gain. Large common-mode signals (within the A1–A2 op amp headroom limits) may be handled at all gains. Finally, because of the symmetry of this configuration, common mode errors in the input amplifiers, if they track, tend to be canceled out by the subtractor output stage. These features explain the popularity of this three-op-amp in amp configuration—it is capable of delivering the highest performance.

The classic three-op-amp configuration has been used in a number of monolithic IC in amps (see References 8 and 9). Besides offering excellent matching between the three internal op amps, thin film laser trimmed resistors provide excellent ratio matching and gain accuracy at much lower cost than using discrete precision op amps and resistor networks. The AD620 (see Reference 10) is an excellent example of monolithic IC in amp technology. A simplified device schematic is shown in Figure 2-13.

The AD620 is a highly popular in amp and is specified for power supply voltages from  $\pm 2.3$  V to  $\pm 18$  V. Input voltage noise is only  $9 \text{ nV}/\sqrt{\text{Hz}}$  @ 1 kHz. Maximum input bias current is only 1 nA, due to the use of superbeta transistors for Q1–Q2.

Overvoltage protection is provided by the internal  $400 \Omega$  thin-film current-limit resistors in conjunction with the diodes connected from the emitter-to-base of Q1 and Q2. The gain  $G$  is set with a single external  $R_G$  resistor, as noted by Eq. 2-4.

$$G = (49.4 \text{ k}\Omega / R_G) + 1 \quad \text{Eq. 2-4}$$

As can be noted from this expression and Figure 2-13, the AD620 internal resistors are trimmed so that standard 1% or 0.1% resistors can be used to set gain to popular values.

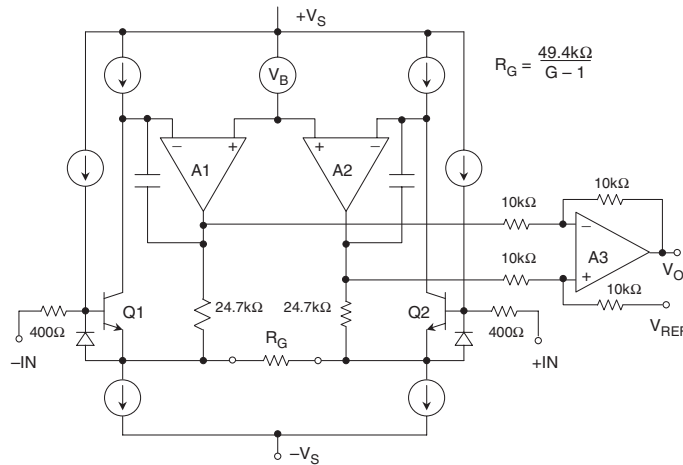


Figure 2-13: The AD620 in amp simplified schematic

As is true in the case of the two-op-amp in amp configuration, single supply operation of the three-op-amp in amp requires an understanding of the internal node voltages. Figure 2-14 shows a generalized diagram of the in amp operating on a single 5 V supply. The maximum and minimum allowable output voltages of the individual op amps are designated  $V_{OH}$  (maximum high output) and  $V_{OL}$  (minimum low output), respectively.

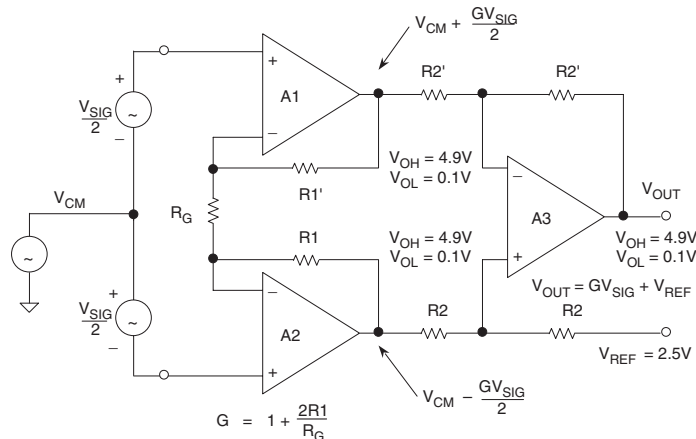


Figure 2-14: Three-op-amp in amp single 5 V supply restrictions

Note that the gain from the common-mode voltage to the outputs of A1 and A2 is unity. It can be stated that *the sum of the common-mode voltage and the signal voltage at these outputs must fall within the amplifier output voltage range*. Obviously this configuration cannot handle input common-mode voltages of either zero volts or 5 V, because of saturation of A1 and A2. As in the case of the two-op-amp in amp, the output reference is positioned halfway between  $V_{OH}$  and  $V_{OL}$  to allow for bipolar differential input signals.

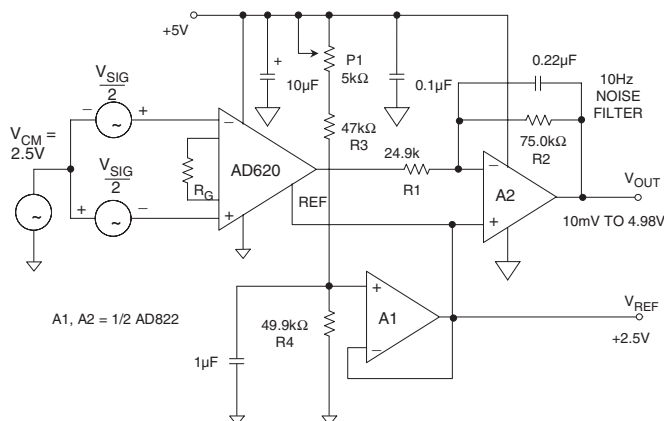
While there are a number of good single-supply in amps, such as the AD627 discussed above, the highest performance devices are still among those specified for traditional dual-supply operation, i.e., the

just-discussed AD620. For certain applications, even such devices as the AD620, which has been designed for dual supply operation, can be used with full precision on a single-supply power system.

### Precision Single-Supply Composite In Amp

One way to achieve both high precision and single-supply operation takes advantage of the fact that many popular sensors (e.g. strain gauges) provide an output signal that is inherently centered around an approximate mid-point of the supply voltage (and/or the reference voltage). Taking advantage of this basic point allows the inputs of a signal conditioning in amp to be biased at “mid-supply.” As a consequence of this step, the inputs needn’t operate near ground or the positive supply voltage, and the in amp can still be used with all its precision.

Under these conditions, an AD620 dual-supply in amp referenced to the supply mid-point followed by a rail-to-rail op amp output gain stage provides very high dc precision. Figure 2-15 illustrates one such high performance in amp, which operates on a single 5 V supply.



**Figure 2-15: A precision single-supply composite in amp with rail-to-rail output**

This circuit uses the AD620 as a low-cost precision in amp for the input stage, along with an AD822 JFET-input dual rail-to-rail output op amp for the output stage, comprised of A1 and A2. The output stage operates at a fixed gain of 3, with overall gain set by  $R_G$ .

In this circuit, R3 and R4 form a voltage divider which splits the supply voltage nominally in half to 2.5 V, with fine adjustment provided by a trimming potentiometer, P1. This voltage is applied to the input of A1, an AD822 voltage follower, which buffers it and provides a low impedance source needed to drive the AD620’s reference pin as well as providing the output reference voltage  $V_{REF}$ . *Note that this feature allows a bipolar  $V_{OUT}$  to be measured with respect to this 2.5 V reference (not to GND).* This is despite the fact that the entire circuit operates from a single (unipolar) supply.

The other half of the AD822 is connected as a gain-of-3 inverter, so that it can output  $\pm 2.5$  V, “rail-to-rail,” with only  $\pm 0.83$  V required of the AD620. This output voltage level of the AD620 is well within the AD620’s capability, thus ensuring high linearity for the front end.

The general gain expression for this composite in amp is the product of the gain of the AD620 stage, and the gain of inverting amplifier:

$$\text{GAIN} = \left( \frac{49.4 \text{ k}\Omega}{R_G} + 1 \right) \left( \frac{R_2}{R_1} \right). \quad \text{Eq. 2-5}$$

For this example, an overall gain of 10 is realized with  $R_G = 21.5 \text{ k}\Omega$  (closest standard value). The table shown in Figure 2-16 summarizes various  $R_G$  gain values, and the resulting performance for gains ranging from 10 to 1000.

CIRCUIT GAIN	$R_G$ ( $\Omega$ )	$V_{OS}$ , RTI ( $\mu\text{V}$ )	TC $V_{OS}$ , RTI ( $\mu\text{V}/^\circ\text{C}$ )	NONLINEARITY (ppm) *	BANDWIDTH (kHz)**
10	21.5k	1000	1000	< 50	600
30	5.49k	430	430	< 50	600
100	1.53k	215	215	< 50	300
300	499	150	150	< 50	120
1000	149	150	150	< 50	30

\*Nonlinearity Measured Over Output Range:  $0.1\text{V} < V_{OUT} < 4.90\text{V}$

\*\*Without 10Hz Noise Filter

**Figure 2-16: Performance summary of the 5 V single-supply AD620/AD822 composite in amp**

In this application, the allowable input voltage on either input to the AD620 must lie between 2 V and 3.5 V in order to maintain linearity. For example, at an overall circuit gain of 10, the common-mode input voltage range spans 2.25 V to 3.25 V, allowing room for the  $\pm 0.25 \text{ V}$  full-scale differential input voltage required to drive the output  $\pm 2.5 \text{ V}$  about  $V_{REF}$ .

The inverting configuration was chosen for the output buffer to facilitate system output offset voltage adjustment by summing currents into the A2 stage buffer's feedback summing node. These offset currents can be provided by an external DAC, or from a resistor connected to a reference voltage.

The AD822 rail-to-rail output stage exhibits a very clean transient response (not shown) and a small-signal bandwidth over 100 kHz for gain configurations up to 300. Note that excellent linearity is maintained over 0.1 V to 4.9 V  $V_{OUT}$ .

To reduce the effects of unwanted noise pickup, a filter capacitor is recommended across A2's feedback resistance to limit the circuit bandwidth to the frequencies of interest. This capacitor forms a first order low-pass filter with R2. The corner frequency is 10 Hz as shown, but this may be easily modified. The capacitor should be a high quality film type, such as polypropylene.



## The AD623 In Amp

Like the two-op-amp in amp counterparts discussed previously, three-op-amp in amps require special design attention for wide CM range inputs on single power supplies. The AD623 single supply in amp configuration (see Reference 11), shown below in Figure 2-17 offers an attractive solution. In this device PNP emitter follower level shifters Q1 and Q2 allow the input signal to go 150 mV below the negative supply, and to within 1.5 V of the positive supply. The AD623 is fully specified for both single power supplies between 3 V and +12 V, and dual supplies between  $\pm 2.5$  V and  $\pm 6$  V.

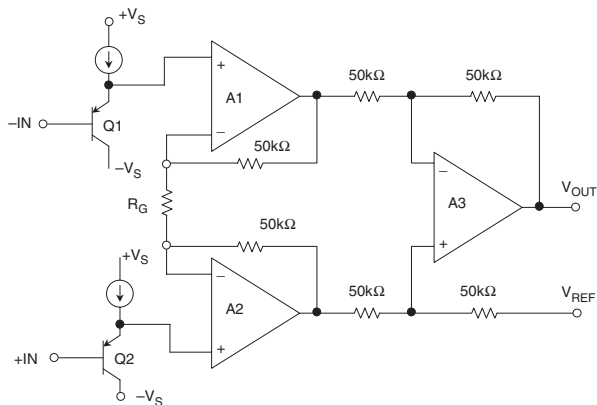


Figure 2-17: AD623 single-supply in amp architecture

The AD623 data sheet (Reference 11, again) contains excellent discussions and data on allowable input/output voltage ranges as a function of gain and power supply voltages. In addition, interactive design tools that perform calculations relating these parameters for a number of in amps, including the AD623, are available on the ADI Web site.

The key specifications of the AD623 are summarized in Figure 2-18.

- Wide Supply Range: +3V to  $\pm 6$ V
- Input Voltage Range:  $-V_S - 0.15$ V to  $+V_S - 1.5$ V
- 575 $\mu$ A Maximum Supply Current
- Gain Range: 1 to 1000
- 100 $\mu$ V Maximum Input Offset Voltage (AD623B)
- 1 $\mu$ V/ $^{\circ}$ C Maximum Offset Voltage TC (AD623B)
- 50ppm Gain Nonlinearity
- 105dB CMR @ 60Hz, 1k $\Omega$  Source Imbalance,  $G \geq 100$
- 3 $\mu$ V p-p 0.1Hz to 10Hz Input Voltage Noise ( $G = 1$ )

Figure 2-18: AD623 in amp key specifications

## In Amp DC Error Sources

The dc and noise specifications for in amps differ slightly from conventional op amps, so some discussion is required in order to fully understand the error sources.

The gain of an in amp is usually set by a single resistor. If the resistor is external to the in amp, its value is either calculated from a formula or chosen from a table on the data sheet, depending on the desired gain.

Absolute value laser wafer trimming allows the user to program gain accurately with this single resistor. The absolute accuracy and temperature coefficient of this resistor directly affects the in amp gain accuracy and drift. Since the external resistor will never exactly match the internal thin film resistor tempcos, a low TC ( $<25$  ppm/ $^{\circ}\text{C}$ ) metal film resistor should be chosen, preferably with a 0.1% or better accuracy.

Often specified as having a gain range of 1 to 1000, or 1 to 10,000, many in amps will work at higher gains, but the manufacturer will not guarantee a specific level of performance at these high gains. In practice, as the gain-setting resistor becomes smaller, any errors due to the resistance of the metal runs and bond wires become significant. These errors, along with an increase in noise and drift, may make higher single-stage gains impractical. In addition, input offset voltages can become quite sizable when reflected to output at high gains. For instance, a 0.5 mV input offset voltage becomes 5 V at the output for a gain of 10,000. For high gains, the best practice is to use an in amp as a preamplifier, then use a post amplifier for further amplification.

In a *pin-programmable-gain* in amp such as the AD621, the gain-set resistors are internal, well matched, and the device gain accuracy and gain drift specifications include their effects. The AD621 is otherwise generally similar to the externally gain-programmed AD620.

The *gain error* specification is the maximum deviation from the gain equation. Monolithic in amps such as the AD624C have very low factory trimmed gain errors, with its maximum error of 0.02% at  $G = 1$  and 0.25% at  $G = 500$  being typical for this high quality in amp. Notice that the gain error increases with increasing gain. Although externally connected gain networks allow the user to set the gain exactly, the temperature coefficients of the external resistors and the temperature differences between individual resistors within the network all contribute to the overall gain error. If the data is eventually digitized and presented to a digital processor, it may be possible to correct for gain errors by measuring a known reference voltage and then multiplying by a constant.

*Nonlinearity* is defined as the maximum deviation from a straight line on the plot of output versus input. The straight line is drawn between the end points of the actual transfer function. Gain nonlinearity in a high quality in amp is usually 0.01% (100 ppm) or less, and is relatively insensitive to gain over the recommended gain range.

The total *input offset voltage* of an in amp consists of two components (see Figure 2-19). *Input* offset voltage,  $V_{OSI}$ , is the input offset component that is reflected to the output of the in amp by the gain  $G$ . *Output* offset voltage,  $V_{OSO}$ , is independent of gain.

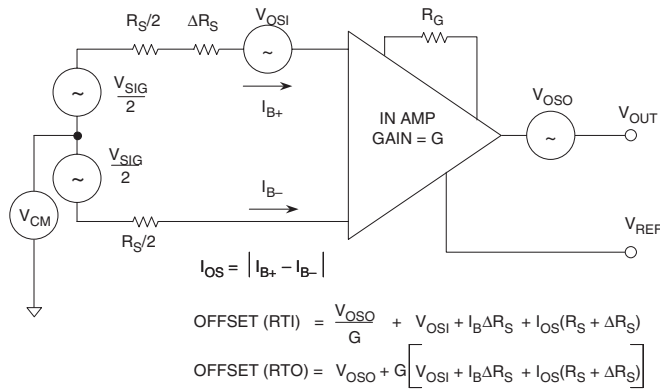


Figure 2-19: In amp offset voltage model

At low gains, output offset voltage is dominant, while at high gains input offset dominates. The output offset voltage drift is normally specified as drift at  $G = 1$  (where input effects are insignificant), while input offset voltage drift is given by a drift specification at a high gain (where output offset effects are negligible).

The total output offset error, referred to the input (RTI), is equal to  $V_{OSI} + V_{OSO}/G$ . In amp data sheets may specify  $V_{OSI}$  and  $V_{OSO}$  separately, or give the total RTI input offset voltage for different values of gain.

*Input bias currents* may also produce offset errors in in amp circuits (Figure 2-19). If the source resistance,  $R_S$ , is unbalanced by an amount,  $\Delta R_S$ , (often the case in bridge circuits), there is an additional input offset voltage error due to the bias current, equal to  $I_B \Delta R_S$  (assuming that  $I_{B+} \approx I_{B-} = I_B$ ). This error is reflected to the output, scaled by the gain  $G$ .

The input offset current,  $I_{OS}$ , creates an input offset voltage error across the source resistance,  $R_S + \Delta R_S$ , equal to  $I_{OS}(R_S + \Delta R_S)$ , which is also reflected to the output by the gain,  $G$ .

In amp *common-mode error* is a function of both gain and frequency. Analog Devices specifies in amp CMR for a 1 k $\Omega$  source impedance unbalance at a frequency of 60 Hz. The RTI common-mode error is obtained by dividing the common-mode voltage,  $V_{CM}$ , by the common-mode rejection ratio, CMRR.

Figure 2-20 shows the CMR for the AD620 in amp as a function of frequency, with a 1 k $\Omega$  source impedance imbalance.

*Power supply rejection* (PSR) is also a function of gain and frequency. For in amps, it is customary to specify the sensitivity to each power supply separately, as shown in Figure 2-21 for the AD620. The RTI power supply rejection error is obtained by dividing the power supply deviation from nominal by the power supply rejection ratio, PSRR.

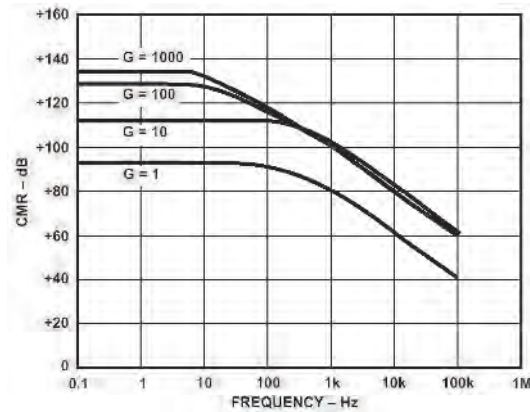


Figure 2-20: AD620 In amp common-mode rejection (CMR) versus frequency for 1 k $\Omega$  source imbalance

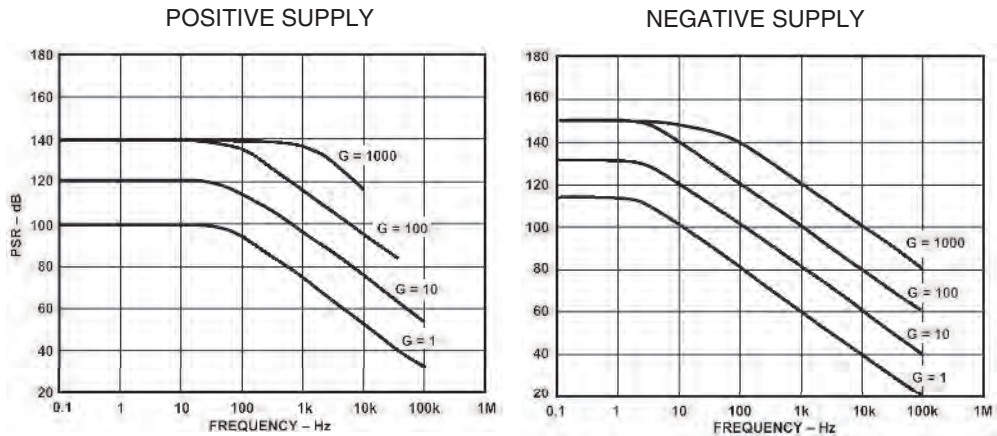


Figure 2-21: AD620 in amp power supply rejection (PSR) versus frequency

Because of the relatively poor PSR at high frequencies, decoupling capacitors are required on both power pins to an in amp. Low inductance ceramic capacitors (0.01  $\mu$ F to 0.1  $\mu$ F) are appropriate for high frequencies. Low ESR electrolytic capacitors should also be located at several points on the PC board for low frequency decoupling.

Note that these decoupling requirements apply to all linear devices, including op amps and data converters. Further details on power supply decoupling are found in Chapter 7.

Now that all dc error sources have been accounted for, a worst case dc error budget can be calculated by reflecting all the sources to the in amp input, as is illustrated by the table of Figure 2-22.

It should be noted that the dc errors can be referred to the in amp output (RTO), by simply multiplying the RTI error by the in amp gain.

ERROR SOURCE	RTI VALUE
Gain Accuracy (ppm)	Gain Accuracy $\times$ FS Input
Gain Nonlinearity (ppm)	Gain Nonlinearity $\times$ FS Input
Input Offset Voltage, $V_{OSI}$	$V_{OSI}$
Output Offset Voltage, $V_{OSO}$	$V_{OSO} \div G$
Input Bias Current, $I_B$ , Flowing in $\Delta R_S$	$I_B \Delta R_S$
Input Offset Current, $I_{OS}$ , Flowing in $R_S$	$I_{OS}(R_S + \Delta R_S)$
Common Mode Input Voltage, $V_{CM}$	$V_{CM} \div CMRR$
Power Supply Variation, $\Delta V_S$	$\Delta V_S \div PSRR$

Figure 2-22: In amp dc errors referred to the input (RTI)

## In Amp Noise Sources

Since in amps are primarily used to amplify small precision signals, it is important to understand the effects of all the associated noise sources. The in amp noise model is shown in Figure 2-23.

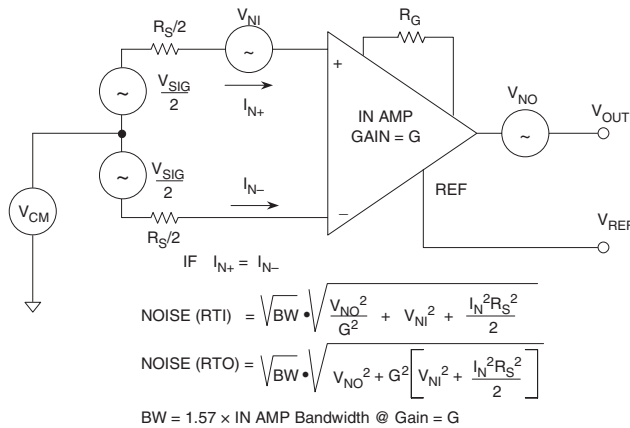


Figure 2-23: In amp noise model

There are two sources of input voltage noise. The first is represented as a noise source,  $V_{NI}$ , in series with the input, as in a conventional op amp circuit. This noise is reflected to the output by the in amp gain,  $G$ . The second noise source is the output noise,  $V_{NO}$ , represented as a noise voltage in series with the in amp output. The output noise, shown here referred to  $V_{OUT}$ , can be referred to the input by dividing by the gain,  $G$ .

There are also two noise sources associated with the input noise currents  $I_{N+}$  and  $I_{N-}$ . Even though  $I_{N+}$  and  $I_{N-}$  are usually equal ( $I_{N+} \approx I_{N-} = I_N$ ), they are *uncorrelated*, and therefore, the noise they each create must be

summed in a root-sum-squares (RSS) fashion.  $I_{N+}$  flows through one-half of  $R_s$ , and  $I_{N-}$  the other half. This generates two noise voltages, each having an amplitude,  $I_N R_s / 2$ . Each of these two noise sources is reflected to the output by the in amp gain,  $G$ .

The total output noise is calculated by combining all four noise sources in an RSS manner:

$$\text{NOISE(RTO)} = \sqrt{BW} \sqrt{V_{NO}^2 + G^2 \left( V_{NI}^2 + \frac{I_{N+}^2 R_s^2}{4} + \frac{I_{N-}^2 R_s^2}{4} \right)} \quad \text{Eq. 2-6}$$

$$\text{If } I_{N+} = I_{N-} = I_N,$$

$$\text{NOISE(RTO)} = \sqrt{BW} \sqrt{V_{NO}^2 + G^2 \left( V_{NI}^2 + \frac{I_N^2 R_s^2}{2} \right)} \quad \text{Eq. 2-7}$$

The total noise, referred to the input (RTI) is simply the above expression divided by the in amp gain,  $G$ :

$$\text{NOISE(RTI)} = \sqrt{BW} \sqrt{\frac{V_{NO}^2}{G^2} + \left( V_{NI}^2 + \frac{I_N^2 R_s^2}{2} \right)} \quad \text{Eq. 2-8}$$

In amp data sheets often present the total voltage noise RTI as a function of gain. This noise spectral density includes both the input ( $V_{NI}$ ) and output ( $V_{NO}$ ) noise contributions. The input current noise spectral density is specified separately.

As in the case of op amps, the total in amp noise RTI must be integrated over the applicable in amp closed-loop bandwidth to compute an RMS value. The bandwidth may be determined from data sheet curves that show frequency response as a function of gain.

Regarding this bandwidth, some care must be taken in computing it, as it is often *not* constant bandwidth product relationship, as is true with VFB op amps. In the case of the AD620 in amp family for example, the gain-bandwidth pattern is more like that of a CFB op amp. In such cases, the safest way to predict the bandwidth at a given gain is to use the curves supplied within the data sheet.

*In Amp Bridge Amplifier Error Budget Analysis*

It is important to understand in amp error sources in a typical application. Figure 2-24 shows a 350 Ω load cell with a full-scale output of 100 mV when excited with a 10 V source. The AD620 is configured for a gain of 100 using the external 499 Ω gain-setting resistor. The table shows how each error source contributes to a total unadjusted error of 2145 ppm. Note, however, that the gain, offset, and CMR errors can all be removed with a system calibration. The remaining errors—gain nonlinearity and 0.1 Hz to 10 Hz noise—cannot be removed with calibration and ultimately limit the system resolution to 42.8 ppm (approximately 14-bit accuracy).

This example is of course just an illustration, but should be useful towards the importance of addressing performance-limiting errors such as gain nonlinearity and LF noise.

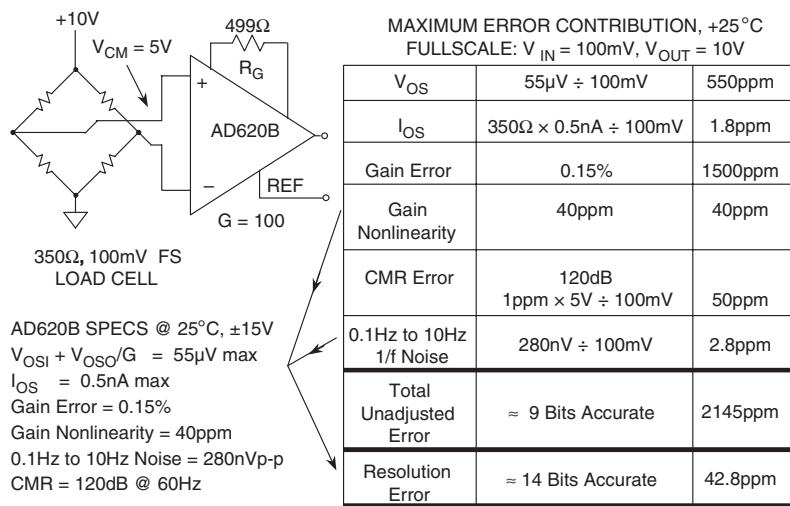


Figure 2-24: AD620B bridge amplifier dc error budget

*In Amp Performance Tables*

Figure 2-25 shows a selection of precision in amps designed primarily for operation on dual supplies. It should be noted that the AD620 is capable of single 5 V supply operation (see Figure 2-15), but neither its input nor its output are capable of rail-to-rail swings.

These tables allow at-a-glance inspection of key errors, which can be critical in getting the most performance from a system. From Figure 2-25 for example, it can be noted that the use of an AD621 in lieu of the AD620B in the gain-of-100 bridge circuit of Figure 2-24 allows reduction of the gain nonlinearity component of error by a factor of four times. It is also important to separate out errors that can be calibrated out as mentioned above, and those that can only be minimized by device specification improvements. Comparison of the AD620B and the AD622 specifications, for example, shows a higher  $V_{OS}$  for the latter. But, since  $V_{OS}$  can be calibrated out, the fact that it is higher for the AD622 isn't material to this particular application. The gain nonlinearity between the AD620 and AD622 is the same, so in an auto-cal system, they would likely perform comparably. On the other hand, the AD621B would be preferable for its lower gain nonlinearity, as noted.

	Gain Accuracy *	Gain Nonlinearity	V <sub>OS</sub> Max	V <sub>OS</sub> TC	CMR Min	0.1Hz to 10Hz p-p Noise
AD524C	0.5% / P	100ppm	50μV	0.5μV/°C	120dB	0.3μV
AD620B	0.5% / R	40ppm	50μV	0.6μV/°C	120dB	0.28μV
AD621B <sup>1</sup>	0.05% / P	10ppm	50μV	1.6μV/°C	100dB	0.28μV
AD622	0.5% / R	40ppm	125μV	1μV/°C	103dB	0.3μV
AD624C <sup>2</sup>	0.25% / R	50ppm	25μV	0.25μV/°C	130dB	0.2μV
AD625C	0.02% / R	50ppm	25μV	0.25μV/°C	125dB	0.2μV
AMP01A	0.6% / R	50ppm	50μV	0.3μV/°C	125dB	0.12μV
AMP02E	0.5% / R	60ppm	100μV	2μV/°C	115dB	0.4μV

\*P = Pin Programmable  
 \*/R = Resistor Programmable

<sup>1</sup> G = 100  
<sup>2</sup> G = 500

**Figure 2-25: Precision in amps: data for V<sub>s</sub> = ±15 V, G = 1000**

In amps specifically designed for single supply operation are also shown, in Figure 2-26. It should be noted that although the specifications in this figure are given for a single 5 V supply, all of the amplifiers are also capable of dual supply operation and are specified for both dual and single supply operation on their data sheets. In addition, the AD623 and AD627 will operate on a single 3 V supply

	Gain Accuracy *	Gain Nonlinearity	V <sub>OS</sub> Max	V <sub>OS</sub> TC	CMR Min	0.1Hz to 10Hz p-p Noise	Supply Current
AD623B	0.5% / R	50ppm	100μV	1μV/°C	105dB	1.5μV	575μA
AD627B	0.35% / R	10ppm	75μV	1μV/°C	85dB	1.5μV	85μA
AMP04E	0.4% / R	250ppm	150μV	3μV/°C	90dB	0.7μV	290μA
AD626B <sup>1</sup>	0.6% / P	200ppm	2.5mV	6μV/°C	80dB	2μV	700μA

\*P = Pin Programmable  
 \*/R = Resistor Programmable

<sup>1</sup> Differential Amplifier, G = 100

**Figure 2-26: Single-supply in amps: data for V<sub>s</sub> = 5 V, G = 1000**

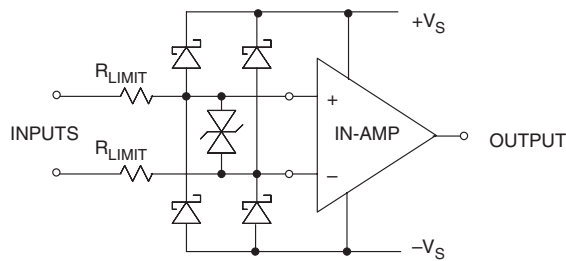
Note that the AD626 is not a true in amp, but is in fact a differential amplifier with a thin-film input attenuator that allows the common-mode voltage to exceed the supply voltages. This device is designed primarily for high- and low-side current-sensing applications. It will also operate on a single 3 V supply.

### ***In Amp Input Overvoltage Protection***

As interface amplifiers for data acquisition systems, in amps are often subjected to input overloads, i.e., voltage levels in excess of the full scale for the selected gain range. The manufacturer's "absolute maximum" input ratings for the device should be closely observed. As with op amps, many in amps have absolute maximum input voltage specifications equal to  $\pm V_s$ .



In some cases, external series resistors (for current limiting) and diode clamps may be used to prevent overload if necessary (see Figure 2-27). Some in amps have built-in overload protection circuits in the form of series resistors. For example, the AD620 series have thin film resistors, and the substrate isolation they provide allows input voltages that can exceed the supplies. Other devices use series-protection FETs; for example, the AMP02 and the AD524, because they act as a low impedance during normal operation, and a high impedance during overvoltage fault conditions. In any instance however, there are always finite safe limits to applied overvoltage (Figure 2-27).



- Always Observe Absolute Maximum Data Sheet Specs
- Schottky Diode Clamps to the Supply Rails Will Limit Input to Approximately  $\pm V_S \pm 0.3V$ , TVSs Limit Differential Voltage
- External Resistors (or Internal Thin-Film Resistors) Can Limit Input Current, but will Increase Noise
- Some In-Amps Have Series-Protection Input FETs for Lower Noise and Higher Input Overvoltages (up to  $\pm 60V$ , Depending on Device)

**Figure 2-27: In amp input overvoltage considerations**

In some instances, an additional Transient Voltage Suppressor (TVS) may be required across the input pins to limit the maximum differential input voltage. This is especially applicable to three-op-amp in amps operating at high gain with low values of  $R_G$ .

A more detailed discussion of input overvoltage and EMI/RFI protection can be found in Chapter 7 of this book.

### ***In Amp Applications***

Some representative in amp applications round out this section, illustrating how the characteristics lend utility and efficiency to a range of circuits.

#### **In Amp Bridge Amplifier**

In amps are widely used as precision signal conditioning elements. A popular application is a bridge amplifier, shown in Figure 2-28. The in amp is ideally suited for this application because the bridge output is fundamentally balanced, and the in amp presents it with a truly balanced high impedance load. The nominal resistor values in the bridge can range from  $100\ \Omega$  to several  $k\Omega$ , but  $350\ \Omega$  is popular for most precision load cells.

Full-scale output voltages from a typical bridge circuit can range from approximately 10 mV to several hundred mV. Typical in amp gains in the order of 100 to 1000 are therefore ideally suited for amplifying these small voltages to levels compatible with popular analog-to-digital converter (ADC) input voltage ranges (usually 1 V to 10 V full scale).

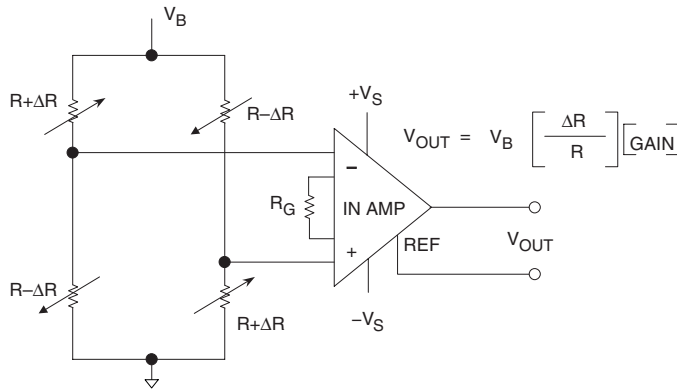


Figure 2-28: Generalized bridge amplifier using an in amp

In addition, the in amp's high CMR at power line frequencies allows common-mode noise to be rejected, when the bridge must be located remotely from the in amp.

Note that a much more thorough discussion of bridge applications can be found in Chapter 4 of this book.

### In Amp A/D Interface

Interfacing bipolar signals to single-supply ADCs presents a challenge. The bipolar signal must be amplified and level-shifted into the input range of the ADC. Figure 2-29 shows how this translation can be achieved using the AD623 in amp, when interfacing a bridge circuit to the AD7776 10-bit, 2.5  $\mu$ s ADC.

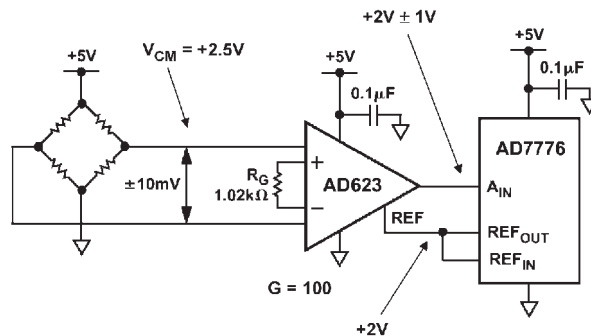


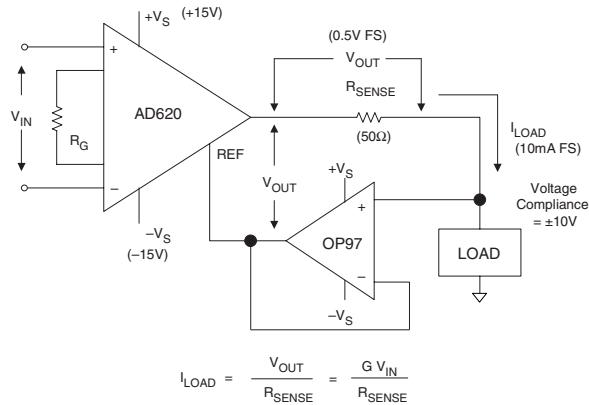
Figure 2-29: Single-supply data acquisition system

The bridge circuit is excited by a 5 V supply. The full-scale output from the bridge ( $\pm 10$  mV) therefore has a common-mode voltage of 2.5 V. The AD623 removes the common-mode component, and amplifies the bridge output by a factor of 100 ( $R_G = 1.02$  k $\Omega$ ).

This results in an output signal swing of  $\pm 1$  V. This signal is level-shifted by connecting the REF pin of the AD623 to the 2 V REF\_OUT of the AD7776 ADC. This sets the common-mode output voltage of the AD623 to 2 V, and the resulting signal into the ADC is  $+2$  V  $\pm 1$  V, corresponding to the input range of the AD7776.

## In Amp Driven Current Source

Figure 2-30 shows a precision voltage-controlled current source using an in amp. The input voltage  $V_{IN}$  develops an output voltage,  $V_{OUT}$ , equal to  $GV_{IN}$  between the output pin of the AD620 and the REF pin. With the connections shown,  $V_{OUT}$  is also applied across sense resistor  $R_{SENSE}$ , thus developing a load current of  $V_{OUT}/R_{SENSE}$ . The OP97 acts as a unity gain buffer to isolate the load from the 20 k $\Omega$  impedance of the REF pin of the AD620. In this circuit the input voltage can be floating with respect to the load ground (as long as there exists a path for the in amp bias currents). The high CMR of the in amp allows high accuracy to be achieved for the load current, despite CM voltages.



**Figure 2-30: Precision voltage-controlled current source using an in amp**

The circuit will work for both large and small values of  $G$  in the AD620. The most simple form would be to let  $G = 1$  with  $R_G$  open. In this case,  $V_{OUT} = V_{IN}$ , and  $I_{LOAD}$  is proportional to  $V_{IN}$ . But the gain factor of the in amp can readily be used to scale almost any input voltage to a desired current level.

The output load voltage compliance is typically  $\pm 10V$  when operating on  $\pm 15V$  power supplies, and load currents up to  $\pm 15mA$  are allowable, limited by the AD620's drive. A typical operating condition might be a full scale load current of 10 mA, a full-scale  $V_{OUT} = 0.5V$ , and  $R_{SENSE} = 50\Omega$ .

For small values of  $R_{SENSE}$ , the OP97 buffer could possibly be eliminated provided the resulting error incurred by the loading effect of the AD620 REF pin is acceptable. In this case the load and bottom  $R_{SENSE}$  node would be connected directly to the in amp REF pin.

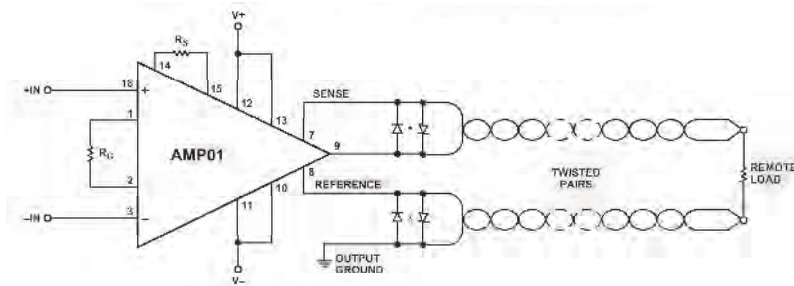
Many other useful variations of the basic circuit exist, and can easily be added. For currents of up to 50 mA, a unity gain, low offset buffer can be added between the AD620 output and the top of  $R_{SENSE}$ . This will remove all load current from the AD620, allowing it to operate with greatest linearity.

The circuit is also very useful at very small currents. It will work well with the OP97 down to around 1  $\mu A$ , before bias current of the op amp becomes a performance limitation. For even lower currents, a precision JFET op amp such as the AD8610 can easily be substituted. This step will allow precise low level currents, down to below 1 nA. Note that the AD8610 must be operated on supplies of  $\pm 13V$  or less, but this isn't necessarily a problem (the AD620 will still operate well on supplies as low as  $\pm 2.5V$ ).

A factor that may not be obvious is that the output current capability of this current source is bilateral, as it is shown. This makes this form of current source a great advantage over a Howland type current source, which are always problematic with the numerous resistors required, which must be well-matched and stable for good performance. In contrast, the current source of Figure 2-30 is clean and efficient, requires no matched resistors, and is precise over very wide current ranges.

### In Amp Remote Load Driver

Often remote loads present a problem in driving, when high accuracy must be maintained at the load end. For this type of requirement, an in amp (or simple differential amplifier) with separate SENSE/FORCE terminals can serve very well, providing a complete solution in one IC. Most of the more popular in amps available today have removed the separate SENSE/FORCE connections, due to the pin limitations of an 8-pin package (AD620, etc.). However, many classic in amps such as the AMP01 do have access to the SENSE/FORCE pins, and can perform remote sensing, as shown in Figure 2-31.



**Figure 2-31: Precision in amp remote load driver using FORCE/SENSE connections**

In this circuit a quad cable composed of two twisted pairs is used. One pair is dedicated to the load HIGH side, the other to the LO side. At the remote end, the load is connected as shown, with each twisted pair terminated at one end of the load.

Although the full load current still flows in the FORCE (AMP01 Pin 9) and OUTPUT GROUND connections, the resulting drop does not create an error, since the remote sensing of the second lead of each pair is returned back to the driver, and carries comparatively very little current. The reverse-parallel connected diodes are optional, and perform a “safety-valve” function, in case a sense line becomes open-circuit (100  $\Omega$  resistors might also be used).

The AMP01 is valuable to this function not simply because of the SENSE/FORCE capability, but because it also is capable of 50 mA output currents and is stable with the capacitive loading presented by a cable. Alternately, a precision differential amplifier like the AMP03 can also be used, at lower current levels.

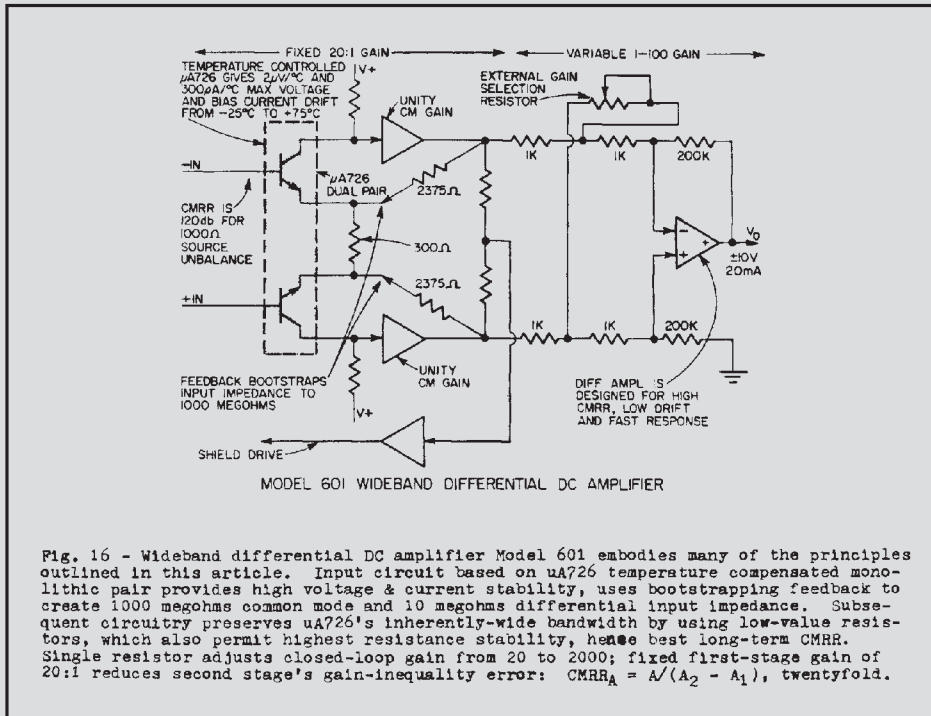
For additional in amp background and reference material, see References 12 through 15.

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## Classic Cameo

## Robert Demrow's "Evolution from Operational Amplifier to Data Amplifier"



As applications engineering manager in the early years of ADI, Robert Demrow published numerous articles and application notes. It is a testament to the quality of these articles that most of them are still germane today—due in no small part to their lucid outlining of fundamental principles.

Demrow's 1968 application note, "Evolution from Operational Amplifier to Data Amplifier" outlined the relevant amplifier operating principles for retrieving analog signals from a noisy environment. It also introduced the ADI Model 601 *data amplifier* (above). Of course, a data amplifier is what we know today as an instrumentation amplifier. Within his Figure 16 can be seen several key operating principles: 1) dual high impedance inputs, as necessary for high CMR, 2) the use of a precision bipolar transistor differential pair front end, for low offset and drift (the  $\mu A726$ ),<sup>1</sup> 3) a balanced, three amplifier stage topology.

It is interesting to note that some more popular IC in amps of 2004 utilize many of the same principles—for example, the AD620 family. Back in 1968, Robert Demrow outlined a host of sound design concepts, leading the way to later solid-state developments and the completely monolithic in amp ICs of today.

<sup>1</sup> James N. Giles, Editor, "The  $\mu A726$  Temperature-Stabilized Transistor Pair," Chapter 8, **Fairchild Semiconductor Linear Integrated Circuits Handbook**, Fairchild Semiconductor, 1967.

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## Programmable Gain Amplifiers

Walt Kester, James Bryant

Most data acquisition systems with wide dynamic range need some method of adjusting the input signal level to the analog-to-digital-converter (ADC). Typical ADC full-scale input voltage ranges lie between 2 V and 10 V. To achieve the rated precision of the converter, the maximum input signal should be fairly near its full-scale voltage.

Transducers, however, have a very wide range of output voltages. High gain is needed for a small sensor voltage, but with a large output, a high gain will cause the amplifier or ADC to saturate. So, some type of predictably controllable gain device is needed. Amplifiers with programmable gain have a variety of applications, and Figure 2-32 lists some of them.

- Instrumentation
- Photodiode circuits
- Ultrasound preamplifiers
- Sonar
- Wide dynamic range sensors
- Driving ADCs (some ADCs have on-chip PGAs)
- Automatic gain control (AGC) loops

**Figure 2-32: Programmable gain amplifier (PGA) applications**

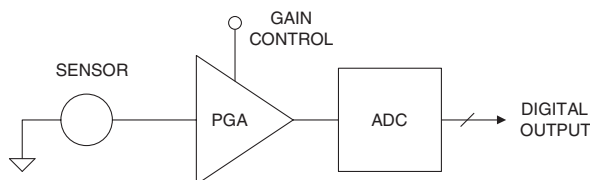
Such a device has a gain that is controlled by a dc voltage or, more commonly, a digital input. This device is known as a *programmable gain amplifier*, or PGA. Typical PGAs may be configured either for selectable *decade gains* such as 10, 100, 1000, etc., or they might also be configured for *binary gains* such as 1, 2, 4, 8, etc. It is a function of the end system of course, which type might be the more desirable.

It should be noted that a factor common to the above application examples is that the different types of signals being handled is diverse. Some may require wide bandwidth, others very low noise, from either high or low impedance sources. The inputs may be single-ended, or they may be differential, crossing over into the realm of the just-discussed in amps.

The output from the PGA may be required to drive some defined input range of an ADC, or it may be part of a smaller subsystem, such as an AGC or gain-ranging loop. The circuits following fall into a range of categories addressing some of these requirements.



A PGA is usually located between a sensor and its ADC, as shown in Figure 2-33. Additional signal conditioning may take place before or after the PGA, depending on the application. For example, a photodiode needs a current-to-voltage converter between it and the PGA. In most other systems, it is better to place the gain first, and condition a larger signal. This reduces errors introduced by the signal conditioning circuitry.



Used to increase the dynamic range of the system

A PGA with a gain of 1 to 2 theoretically increases the dynamic range by 6dB.

A gain of 1 to 4 gives a 12dB increase, etc.

**Figure 2-33: PGAs in data acquisition systems**

To understand the benefits of variable gain, assume an ideal PGA with two settings, gains of one and two. The dynamic range of the system is increased by 6 dB. Increasing the gain to a maximum four results in a 12 dB increase in dynamic range. If the LSB of an ADC is equivalent to 10 mV of input voltage, the ADC cannot resolve smaller signals, but when the gain of the PGA is increased to two, input signals of 5 mV may be resolved.

Thus, a central processor can combine PGA gain information with the digital output of the ADC to increase its resolution by one bit. Essentially, this is the same as adding additional resolution to the ADC. In fact, a number of ADCs now have on-chip PGAs for increased dynamic range (AD77xx-series, for example, covered later).

### PGA Design Issues

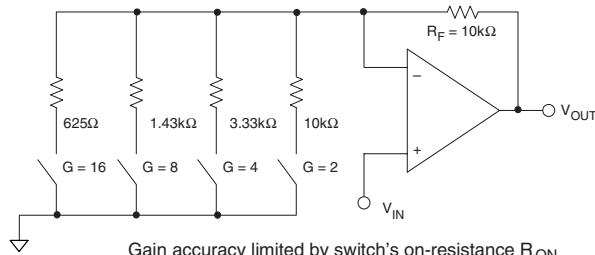
In practice, PGAs aren't ideal, and their error sources must be studied and dealt with. A number of the various PGA design issues are summarized in Figure 2-34.

A fundamental PGA design problem is programming gain accurately. Electromechanical relays have minimal on resistance ( $R_{ON}$ ), but are unsuitable for gain switching—slow, large, and expensive. CMOS switches are small, but they have voltage-/temperature-dependent  $R_{ON}$ , as well as stray capacitance, which may affect PGA ac parameters.

- How to switch the gain
- Effects of the switch on-resistance ( $R_{ON}$ )
- Gain accuracy
- Gain linearity
- Bandwidth versus frequency versus gain
- Dc offset
- Gain and offset drift over temperature
- Settling time after switching gain

**Figure 2-34: PGA design issues**

To understand  $R_{ON}$ 's effect on performance, consider Figure 2-35, a poor PGA design. A noninverting op amp has four different gain-set resistors, each grounded by a switch, with an  $R_{ON}$  of 100  $\Omega$ –500  $\Omega$ . Even with  $R_{ON}$  as low as 25  $\Omega$ , the gain of 16 error would be 2.4%, worse than 8-bits.  $R_{ON}$  also changes over temperature and switch-switch.



Gain accuracy limited by switch's on-resistance  $R_{ON}$  and  $R_{ON}$  modulation

$R_{ON}$  typically 100 – 500 $\Omega$  for CMOS or JFET switch

Even for  $R_{ON} = 25\Omega$ , there is a 2.4% gain error for  $G = 16$

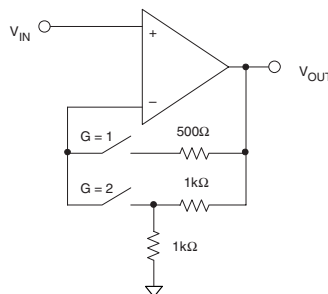
$R_{ON}$  drift over temperature limits accuracy

Must use very low  $R_{ON}$  switches (relays)

**Figure 2-35: A poorly designed PGA**

To attempt “fixing” this design, the resistors might be increased, but noise and offset could then be a problem. The only way to accuracy with this circuit is to use relays, with virtually no  $R_{ON}$ . Only then will the few m $\Omega$  of relay  $R_{ON}$  be a small error vis-à-vis 625  $\Omega$ .

It is much better to use a circuit *insensitive* to  $R_{ON}$ . In Figure 2-36, the switch is placed in series with the inverting input of an op amp. Since the op amp input impedance is very large, the switch  $R_{ON}$  is now irrelevant, and gain is now determined solely by the external resistors. Note:  $R_{ON}$  may add a small offset error if op amp bias current is high (if this is the case, it can readily be compensated with an equivalent resistance at  $V_{IN}$ ).



- $R_{ON}$  is not in series with gain setting resistors
- $R_{ON}$  is small compared to input impedance
- Only slight offset errors occur due to bias current flowing through the switches

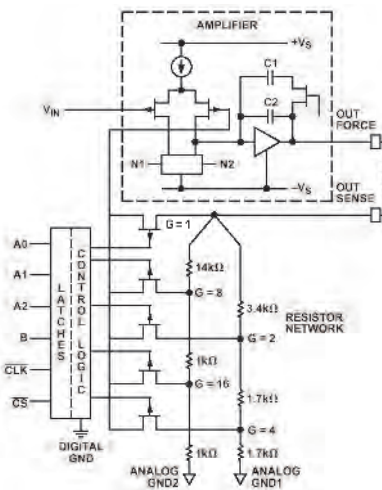
**Figure 2-36: Alternate PGA configuration minimizes the effects of  $R_{ON}$**

## PGA Applications

The following section illustrates several PGA circuits using the above and other concepts.

### AD526 Software Programmable PGA

The AD526 amplifier uses the just-described PGA architecture, integrating it onto a single chip, as diagrammed in Figure 2-37 (see References 1 and 2). The AD526 has five binary gain settings from 1 to 16, and its internal JFET switches are connected to the inverting input of the amplifier as in Figure 2-37. The gain resistors are laser trimmed, providing a maximum gain error of only 0.02%, and a linearity of 0.001%. The use of the FORCE/SENSE terminals connected at the load ensures highest accuracy (it also allows the use of an optional unity-gain buffer, for low impedance loads).



**Figure 2-37: AD526 software programmable PGA simplified schematic**

Functionally speaking, the AD526 is a programmable, precision, noninverting op amp gain stage, logic programmable over a range of 1 to 16 times  $V_{IN}$ . It typically operates from a  $\pm 15$  V power supply, and has  $\pm 10$  V output range (like a conventional op amp).

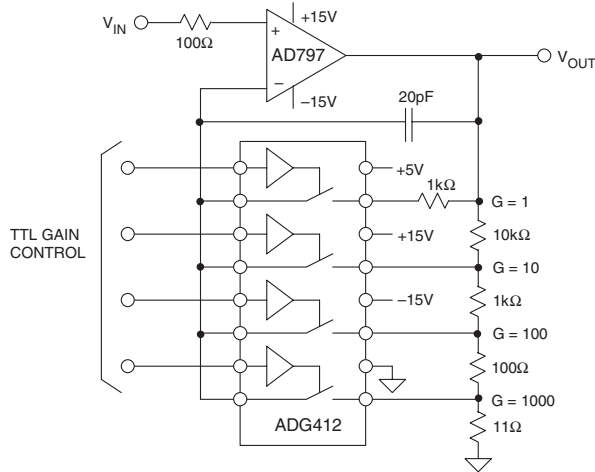
The key specifications for the AD526 are summarized in Figure 2-38.

- Software programmable binary gains from 1 to 16
- Low bias current JFET input stage
- Worst-case gain error: 0.02% (12-bit performance)
- Maximum gain nonlinearity: 0.001%
- Gain change settling time:  $5.6\mu\text{s}$  ( $G = 16$ )
- Small signal bandwidth: 4MHz ( $G = 1$ ), 0.35MHz ( $G = 16$ )
- Latched TTL-compatible control inputs

**Figure 2-38: AD526 PGA key specifications**

## Low Noise PGA

This same design concepts can be used to build a low noise PGA as shown in Figure 2-39. It uses a single op amp, a quad switch, and precision resistors. The lower noise AD797 replaces the JFET input op amp of the AD526, but almost any voltage feedback op amp could be used in this circuit. The ADG412 was picked for its  $R_{ON}$  of  $35\ \Omega$ .



**Figure 2-39: A very low noise PGA using the AD797 and the ADG412**

The resistors were chosen to give decade gains of 1, 10, 100, and 1000, but if other gains are required, the resistor values may easily be altered. Ideally, a single trimmed resistor network should be used both for initial gain accuracy and for low drift over temperature. The 20 pF feedback capacitor ensures stability and holds the output voltage when the gain is switched. The control signal to the switches turns one switch off a few nanoseconds before the second switch turns on. During this break, the op amp is open-loop. Without the capacitor the output would start slewing. Instead, the capacitor holds the output voltage during switching. Since the time that both switches are open is very short, only 20 pF is needed. For slower switches, a larger capacitor may be necessary.

The PGA's input voltage noise spectral density at a gain of 1000 is only  $1.65\text{ nV}/\sqrt{\text{Hz}}$  at 1 kHz, only slightly higher than the noise performance of the AD797 alone. The increase is due to the ADG412 noise, and the current noise of the AD797 flowing through  $R_{ON}$ .

The accuracy of the PGA is important in determining the overall accuracy of a system. The AD797 has a bias current of  $0.9\ \mu\text{A}$ , which, flowing in a  $35\ \Omega$   $R_{ON}$ , results in an additional offset error of  $31.5\ \mu\text{V}$ . Combined with the AD797 offset, the total  $V_{OS}$  becomes  $71.5\ \mu\text{V}$  (max). Offset temperature drift is affected by the change in bias current and  $R_{ON}$ . Calculations show that the total temperature coefficient increases from  $0.6\ \mu\text{V}/^\circ\text{C}$  to  $1.6\ \mu\text{V}/^\circ\text{C}$ . Note that while these errors are small (and may not matter in the end) it is still important to be aware of them.

In practice, circuit accuracy and gain TC will be determined by the external resistors. Input characteristics such as common mode range and input bias current are determined solely by the AD797. A performance summary is shown below in Figure 2-40.

- $R_{ON}$  adds additional input offset and drift:
  - $\Delta V_{OS} = I_b R_{ON} = (0.9\mu A)(35\Omega) = 31.5\mu V$  (max)
  - Total  $V_{OS} = 40\mu V + 31.5\mu V = 71.5\mu V$  (max)
- Temperature drift due to  $R_{ON}$ :
  - At  $+85^\circ C$ ,  $\Delta V_{OS} = (2\mu A)(45\Omega) = 90\mu V$  (max)
- Temperature coefficient total:
  - $\Delta V_{OS} / \Delta T = 0.6\mu V/^\circ C + 1.0\mu V/^\circ C = 1.6\mu V/^\circ C$  (max)
  - Note:  $0.6\mu V/^\circ C$  is due to the AD797B
- RTI Noise :  $1.65nV/\sqrt{Hz}$  @ 1kHz,  $G = 1000$
- Gain switching time  $< 1\mu s$ ,  $G = 10$

Figure 2-40: AD797/ADG412 PGA performance summary

## DAC Programmed PGA

Another PGA configuration uses a DAC in the feedback loop of an op amp to adjust the gain under digital control, as shown in Figure 2-41. The digital code of the DAC controls its attenuation with respect to its reference input  $V_{REF}$ , acting functionally similar to a potentiometer. Attenuating the feedback signal increases the closed-loop gain.

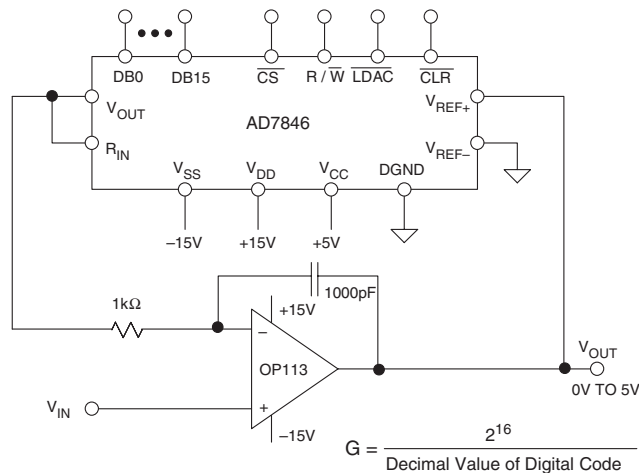


Figure 2-41: Binary gain PGA using a DAC in the feedback path of an op amp

A noninverting PGA of this type requires a multiplying DAC with a voltage mode output. Note that a multiplying DAC is a DAC with a wide reference voltage range, *which includes zero*. For most applications of the PGA, the reference input must be capable of handling bipolar signals. The AD7846 is a 16-bit converter that meets these requirements. In this application, it is used in the standard 2-quadrant multiplying mode.

The OP113 is a low drift, low noise amplifier, but the choice of the amplifier is flexible, and depends on the intended application. The input voltage range depends on the output swing of the AD7846, which is 3 V less than the positive supply, and 4 V above the negative supply. A 1000 pF capacitor is used in the feed-back loop for stability.

The gain of the circuit is set by adjusting the digital inputs of the DAC, according to the equation given in Figure 2-41.  $D_{0-15}$  represents the decimal value of the digital code. For example, if all the bits were set high, the gain would be  $65,536/65,535 = 1.000015$ . If the eight least significant bits are set high and the rest low, the gain would be  $65,536/255 = 257$ . The bandwidth of the circuit is a fairly high 4 MHz for a gain of +1. However, this does reduce with gain, and for a gain of 256, the bandwidth is only 600 Hz. If the gain-bandwidth product were constant, the bandwidth in a gain of 256 should be 15.6 kHz; but the internal capacitance of the DAC reduces the bandwidth to 600 Hz.

Performance characteristics of this binary PGA are summarized in Figure 2-42.

- Gain Accuracy:
  - 0.003% ( $G = +1$ )
  - 0.1% ( $G = +256$ )
- Nonlinearity: 0.001% ( $G = 1$ )
- Offset: 100  $\mu$ V
- Noise: 50 nV/ $\sqrt{\text{Hz}}$
- Bandwidth:
  - 4 MHz ( $G = +1$ )
  - 600 Hz ( $G = +256$ )

**Figure 2-42: Binary gain PGA performance**

The gain accuracy of the circuit is determined by the resolution of the DAC and the gain setting. At a gain of 1, all bits are on, and the accuracy is determined by the DNL specification of the DAC, which is  $\pm 1$  LSB maximum. Thus, the gain accuracy is equivalent to 1 LSB in a 16-bit system, or 0.003%.

However, as the gain is increased, fewer of the bits are on. For a gain of 256, only bit 8 is turned on. The gain accuracy is still dependent on the  $\pm 1$  LSB of DNL, but now that is compared to only the lowest eight bits. Thus, the gain accuracy is reduced to 1 LSB in an 8-bit system, or 0.4%. If the gain is increased above 256, the gain accuracy is reduced further. The designer must determine an acceptable level of accuracy. In this particular circuit, the gain was limited to 256.

## Differential Input PGAs

There are often applications where a PGA with differential inputs is needed, instead of the single-ended types discussed so far. The AD625 combines an instrumentation amplifier topology similar to the AD620 with external gain switching capabilities to accomplish 12-bit gain accuracy (see Reference 3). An external switch is needed to switch between different gain settings, but its on resistance does not significantly affect the gain accuracy due to the unique design of the AD625.

The circuit in Figure 2-43 uses an ADG409 CMOS switch to switch the connections to an external gain-setting resistor network. In the example shown, resistors were chosen for gains of 1, 4, 16, and 64. Other features of the AD625 are 0.001% nonlinearity, wide bandwidth, and very low input noise.

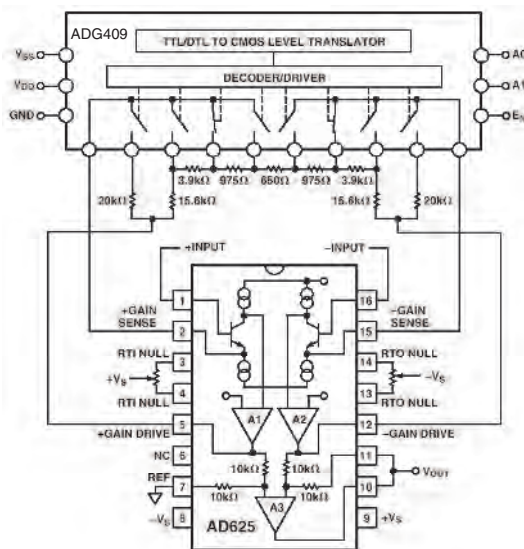


Figure 2-43: A software-programmable gain amplifier

The AD625 is uniquely designed so that the on resistance of the switches does not introduce significant error in the circuit. This can be understood by considering the simplified AD625 circuit shown Figure 2-44. The voltages shown are for an input of +1 mV on +IN and 0 V on -IN. The gain is set to 64 with  $R_G = 635 \Omega$  and the two resistors,  $R_F = 20 \text{ k}\Omega$ .

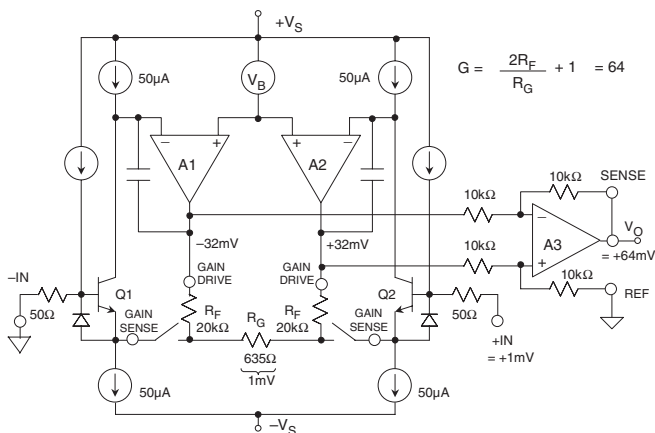
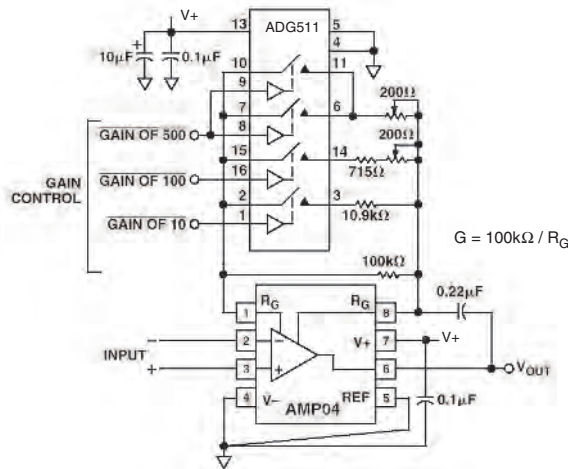


Figure 2-44: AD625 details showing external switches and gain-setting resistors for  $R_G = 635 \Omega$ , +IN = 1 mV, -IN = 0 V

Since transistors Q1 and Q2 have 50  $\mu\text{A}$  current sources in both their emitters and their collectors, negative feedback around A1 and A2, respectively, will ensure that no net current flows through either *gain sense* pin into either emitter. Since no current flows in the gain sense pins, no current flows in the gain setting switches, and their  $R_{\text{ON}}$  does not affect either gain or offset. In real life there will be minor mismatches, but the errors are well under the 12-bit level.

The differential gain between the inputs and the A1-A2 outputs is  $2R_F/R_G + 1$ . The unity-gain difference amplifier and matched resistors removes CM voltage, and drives the output.

Noninverting PGA circuits using an op amp are easily adaptable to single supply operation, but when differential inputs are desired, a single-supply in amp such as the AD623, AD627, or the AMP04 should be used. The AMP04 is used with an external CMOS switch in the single supply in amp PGA shown in Figure 2-45.



**Figure 2-45: Single supply instrumentation PGA using the AMP04 in amp and the ADG511 switch**

This circuit has selectable gains of 1, 10, 100, and 500, which are controlled by an ADG511. The ADG511 was chosen as a single supply switch with a low  $R_{\text{ON}}$  of 45  $\Omega$ . A disadvantage of this circuit is that the gain of this circuit is dependent on the  $R_{\text{ON}}$  of the switches. Trimming is required at the higher gains to achieve accuracy. At a gain of 500, two switches are used in parallel, but their resistance causes a 10% gain error in the absence of adjustment.

## ADC with Onboard PGA

Certain ADCs (such as the AD77ss measurement series) have built-in PGAs and other conditioning circuitry. Circuit design with these devices is much easier, because an external PGA and its control logic are not needed. Furthermore, all the errors of the PGA are included in the specifications of the ADC, making error calculations simple.

The PGA gain is controlled over the common ADC serial interface, and the gain setting is factored into the conversion, saving additional calculations to determine input voltage.



This combination of ADC and PGA is very powerful and enables the realization of a highly accurate system, with a minimum of circuit design. As an example, Figure 2-46 shows a simplified diagram of the AD7730 sigma-delta measurement ADC which is optimized for digitizing low voltage bridge outputs directly (as low as 10 mV full scale) to greater than 16 bits noise free code resolution, without the need for external signal conditioning circuits.

Additional information and background reading on PGAs can be found in References 4 and 5.

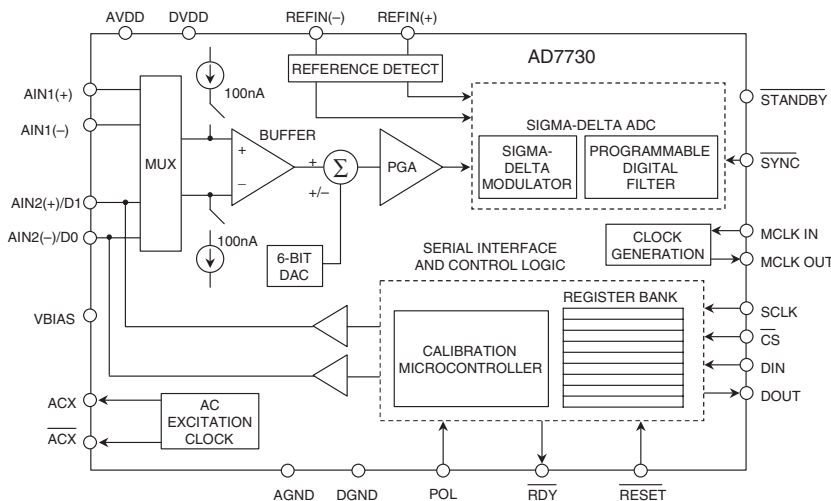


Figure 2-46: AD7730 sigma-delta measurement ADC with on-chip PGA

## References: Programmable Gain Amplifiers

1. John Krehbiel, "Monolithic Software Programmable-Gain Amplifier," *Analog Dialogue*, Vol. 21, No. 2, 1987, pp. 12–13.
2. Data sheet for **AD526 Software Programmable Gain Amplifier**, [www.analog.com](http://www.analog.com).
3. Data sheet for **AD625 Programmable Gain Instrumentation Amplifier**, [www.analog.com](http://www.analog.com).
4. Chapters 2, 3, 8, Walt Kester, Editor, **Practical Design Techniques for Sensor Signal Conditioning**, Analog Devices, 1999, ISBN: 0-916550-20-6.
5. Chapter 2, Walt Kester, Editor, **Linear Design Seminar**, Analog Devices, 1995, ISBN: 0-916550-15-X.

## Isolation Amplifiers

Walt Kester, James Bryant

### Analog Isolation Techniques

There are many applications where it is desirable, or even essential, for a sensor to have no direct (“galvanic”) electrical connection with the system to which it is supplying data. This might be in order to avoid the possibility of dangerous voltages or currents from one half of the system doing damage in the other, or to break an intractable ground loop. Such a system is said to be “isolated,” and the arrangement that passes a signal without galvanic connections is known as an *isolation barrier*.

The protection of an isolation barrier works in both directions, and may be needed in either, or even in both. The obvious application is where a sensor may accidentally encounter high voltages, and the system it is driving must be protected. Or a sensor may need to be isolated from accidental high voltages arising downstream in order to protect its environment. Examples include the need to prevent the ignition of explosive gases by sparks at sensors and the protection from electric shock of patients whose ECG, EEG, or EMG is being monitored. The ECG case is interesting, as protection may be required in *both* directions: the patient must be protected from accidental electric shock, but if the patient’s heart should stop, the ECG machine must be protected from the very high voltages (>7.5 kV) applied to the patient by the defibrillator that will be used to attempt to restart it. A summary of applications for isolation amplifiers (both analog and digital) is shown in Figure 2-47.

- Sensor is at a High Potential Relative to Other Circuitry  
(or may become so under Fault Conditions)
- Sensor May Not Carry Dangerous Voltages, Irrespective  
of Faults in Other Circuitry  
(e.g. Patient Monitoring and Intrinsically Safe Equipment  
for use with Explosive Gases)
- To Break Ground Loops

**Figure 2-47: Applications for isolation amplifiers**

Just as interference, or *unwanted* information, may be coupled by electric or magnetic fields, or by electromagnetic radiation, these phenomena may be used for the transmission of *wanted* information in the design of isolated systems.

The most common isolation amplifiers use *transformers*, which exploit magnetic fields, and another common type uses small high voltage capacitors, exploiting electric fields. *Optoisolators*, which consist of an LED and a photocell, provide isolation by using light, a form of electromagnetic radiation. Different isolators have differing performance: some are sufficiently linear to pass high accuracy analog signals across an isolation barrier. With others, the signal may need to be converted to digital form before transmission for accuracy is to be maintained (note this is a common V/F converter application).

Transformers are capable of analog accuracy of 12 to 16 bits and bandwidths up to several hundred kHz; their maximum voltage rating rarely exceeds 10 kV, and is often much lower. *Capacitively-coupled* isolation amplifiers have lower accuracy, perhaps 12 bits maximum, lower bandwidth, and lower voltage ratings—but they are low cost. Optical isolators are fast and cheap, and can be made with very high voltage ratings (4 kV – 7 kV is one of the more common ratings), but they have poor analog domain linearity and are not usually suitable for direct coupling of precision analog signals.

Linearity and isolation voltage are not the only issues to be considered in the choice of isolation systems. Operating power is of course, essential. Both the input and the output circuitry must be powered and, unless there is a battery on the isolated side of the isolation barrier (which is possible, but rarely convenient), some form of isolated power must be provided. Systems using transformer isolation can easily use a transformer (either the signal transformer or another one) to provide isolated power. It is, however, impractical to transmit useful amounts of power by capacitive or optical means. Systems using these forms of isolation must make other arrangements to obtain isolated power supplies—this is a powerful consideration in favor of choosing transformer-isolated isolation amplifiers: they almost invariably include an isolated power supply.

The isolation amplifier has an input circuit that is galvanically isolated from the power supply and the output circuit. In addition, there is minimal capacitance between the input and the rest of the device. Therefore, there is no possibility for dc current flow and minimum ac coupling. Isolation amplifiers are intended for applications requiring safe, accurate measurement of low frequency voltage or current (up to about 100 kHz) in the presence of high common-mode voltage (to thousands of volts) with high common-mode rejection. They are also useful for line-receiving of signals transmitted at high impedance in noisy environments, and for safety in general-purpose measurements, where dc and line-frequency leakage must be maintained at levels well below certain mandated minimums. Principal applications are in electrical environments of the kind associated with medical equipment, conventional and nuclear power plants, automatic test equipment, and industrial process control systems.

### AD210 Three-Port Isolator

In a basic two-port form of isolator, the output and power circuits are not isolated from one another. A *three-port isolator* (input, power, output) is shown in Figure 2-48. Note that in this diagram, the input circuits, output circuits, and power source are all isolated from one another. This figure represents the circuit architecture of a self-contained isolator, the AD210 (see References 1 and 2).

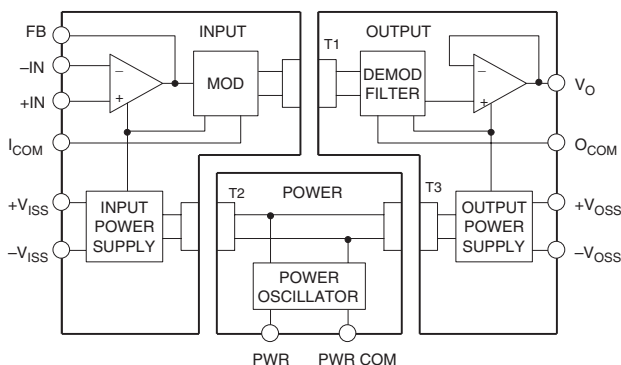


Figure 2-48: AD210 three-port isolation amplifier

An isolator of this type requires power from a two-terminal dc power supply (PWR, PWR COM). An internal oscillator (50 kHz) converts the dc power to ac, which is transformer-coupled to the shielded input section, then converted to dc for the input stage and the auxiliary power output.

The ac carrier is also modulated by the input stage amplifier output, transformer-coupled to the output stage, demodulated by a phase-sensitive demodulator (using the carrier as the reference), filtered, and buffered using isolated dc power derived from the carrier. The AD210 allows the user to select gains from 1 to 100, using external resistors with the input section op amp. Bandwidth is 20 kHz, and voltage isolation is 2500 V rms (continuous) and  $\pm 3500$  V peak (continuous).

The AD210 is a three-port isolation amplifier, thus the power circuitry is isolated from both the input and the output stages and may therefore be connected to either (or to neither), without change in functionality. It uses transformer isolation to achieve 3500 V isolation with 12-bit accuracy.

Key specifications for the AD210 are summarized in Figure 2-49.

- Transformer Coupled
- High Common-Mode Voltage Isolation:
  - 2500V RMS Continuous
  - $\pm 3500$ V Peak Continuous
- Wide Bandwidth: 20kHz (Full Power)
- 0.012% Maximum Linearity Error
- Input Amplifier: Gain 1 to 100
- Isolated Input and Output Power Supplies,  $\pm 15$ V,  $\pm 5$ mA

**Figure 2-49: AD210 isolation amplifier key specifications**

## Motor Control Isolation Amplifier

A typical isolation amplifier application using the AD210 is shown in Figure 2-50. The AD210 is used with an AD620 instrumentation amplifier in a current-sensing system for motor control. The input of the AD210, being isolated, can be directly connected to a 110 V or 230 V power line without protection being necessary. The input section's isolated  $\pm 15$  V powers the AD620, which senses the voltage drop in a small value current sensing resistor. The AD210 input stage op amp is simply connected as a unity-gain follower, which minimizes its error contribution. The 110 V or 230 V rms common-mode voltage is ignored by this isolated system.

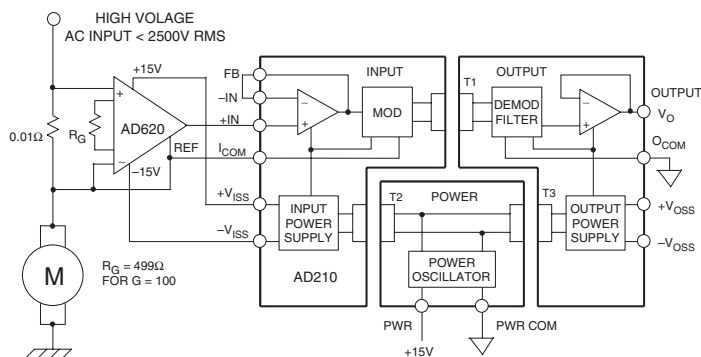


Figure 2-50: Motor control current sensing

Within this system the AD620 preamp is used as the system scaling control point, and will produce and output voltage proportional to motor current, as scaled by the sensing resistor value and gain as set by the AD620's  $R_G$ . The AD620 also improves overall system accuracy, as the AD210  $V_{OS}$  is 15 mV, versus the AD620's 30  $\mu$ V (with less drift also). Note that if higher dc offset and drift are acceptable, the AD620 may be omitted and the AD210 connected at a gain of 100.

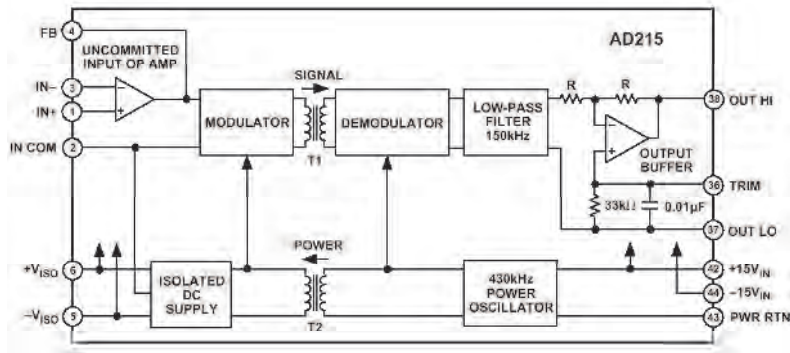
## Optional Noise Reduction Post Filter

Due to the nature of this type of carrier-operated isolation system, there will be certain operating situations where some residual ac carrier component will be superimposed upon the recovered output dc signal. When this occurs, a low impedance passive RC filter section following the output stage may be used (if the following stage has a high input impedance, i.e., nonloading to this filter). Note that will be the case for many high input impedance sampling ADCs, which appear essentially as a small capacitor. A 150  $\Omega$  resistance and 1 nF capacitor will provide a corner frequency of about 1 kHz. Note also that the capacitor should be a film type for low errors, such as polypropylene.

## AD215 Two-Port Isolator

The AD215 is a high speed, two-port isolation amplifier, designed to isolate and amplify wide bandwidth analog signals (see Reference 3). The innovative circuit and transformer design of the AD215 ensures wide-band dynamic characteristics, while preserving dc performance specifications. An AD215 block diagram is shown in Figure 2-51.

The AD215 provides complete galvanic isolation between the input and output of the device, which also includes the user-available front-end isolated bipolar power supply. The functionally complete design,



**Figure 2-51: AD215 120kHz low distortion two-port isolation amplifier**

powered by a  $\pm 15$  V dc supply on the output side, eliminates the need for a user supplied isolated dc/dc converter. This permits the designer to minimize circuit overhead and reduce overall system design complexity and component costs.

The design of the AD215 emphasizes maximum flexibility and ease of use in a broad range of applications where fast analog signals must be measured under high common-mode voltage (CMV) conditions.

The AD215 has a  $\pm 10$  V input/output range, a specified gain range of 1 V/V to 10 V/V, a buffered output with offset trim and a user-available isolated front end power supply which produces  $\pm 15$  V dc at  $\pm 10$  mA. The key specifications of the AD215 are summarized in Figure 2-52.

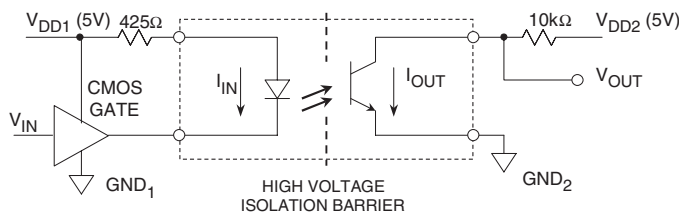
- Isolation voltage: 1500V rms
- Full power bandwidth: 120kHz
- Slew rate: 6V/ $\mu$ s
- Harmonic distortion:  $-80$ dB @ 1kHz
- 0.005% maximum linearity error
- Gain range: 1 to 10
- Isolated input power supply:  $\pm 15$ V @  $\pm 10$ mA

**Figure 2-52: AD215 isolation amplifier key specifications**

## Digital Isolation Techniques

Analog isolation amplifiers find many applications where a high isolation is required, such as in medical instrumentation. Digital isolation techniques provide similar galvanic isolation, and are a reliable method of transmitting digital signals without ground noise.

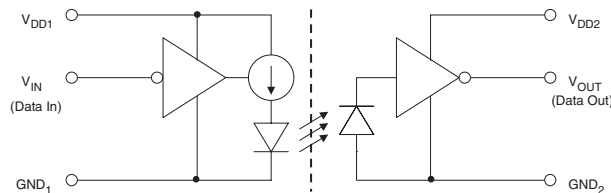
Optocouplers (also called optoisolators) are useful and available in a wide variety of styles and packages. A typical optocoupler based on an LED and a phototransistor is shown in Figure 2-53. A current of approximately 10 mA drives an LED transmitter, with light output is received by a phototransistor. The light produced by the LED saturates the phototransistor. Input/output isolation of 5000 V rms to 7000 V rms is common. Although fine for digital signals, optocouplers are too nonlinear for most analog applications. Also, since the phototransistor is being saturated, response times can range from 10  $\mu$ s to 20  $\mu$ s in slower devices, limiting high speed applications.



- Uses Light for Transmission over a High Voltage Barrier
- The LED is the Transmitter, and the Phototransistor is the Receiver
- High Voltage Isolation: 5000V to 7000V rms
- Nonlinear — Best for Digital or Frequency Information
- Rise and Fall times can be 10 $\mu$ s to 20 $\mu$ s in Slower Devices
- Example: Siemens ILQ-1 Quad ([www.siemens.com](http://www.siemens.com))

**Figure 2-53: Digital isolation using LED/phototransistor optocouplers**

A much faster optocoupler architecture is shown in Figure 2-54, and is based on an LED and a photodiode. The LED is again driven with a current of approximately 10 mA.



- 5V Supply Voltage
- 2500V rms I/O Withstand Voltage
- Logic Signal Frequency: 12.5MHz Maximum
- 25MBd Maximum Data Rate
- 40ns Maximum Propagation Delay
- 9ns Typical Rise/Fall Time
- Example: Agilent HCPL-7720
- ([www.semiconductor.agilent.com](http://www.semiconductor.agilent.com))

**Figure 2-54: Digital isolation using LED/photodiode optocouplers**

This produces a light output sufficient to generate enough current in the receiving photodiode to develop a valid high logic level at the output of the transimpedance amplifier. Speed can vary widely between opto-couplers, and the fastest ones have propagation delays of 20 ns typical, and 40 ns maximum, and can handle data rates up to 25 MBd for NRZ data. This corresponds to a maximum square wave operating frequency of 12.5 MHz, and a minimum allowable passable pulse width of 40 ns.

### AD260/AD261 High Speed Logic Isolators

The AD260/AD261 family of digital isolators operates on a principle of transformer-coupled isolation (see Reference 4). They provide isolation for five digital control signals to/from high speed DSPs, microcontrollers, or microprocessors. The AD260 also has a 1.5 W transformer for a 3.5 kV rms isolated external dc/dc power supply circuit.

Each line of the AD260 can handle digital signals up to 20 MHz (40 MBd) with a propagation delay of only 14 ns which allows for extremely fast data transmission. Output waveform symmetry is maintained to within  $\pm 1$  ns of the input so the AD260 can be used to accurately isolate time-based pulsewidth modulator (PWM) signals.

A simplified schematic of one channel of the AD260/AD261 is shown in Figure 2-55. The data input is passed through a Schmitt trigger circuit, through a latch, and a special transmitter circuit which differentiates the edges of the digital input signal and drives the primary winding of a proprietary transformer with a “set-high/set-low” signal. The secondary of the isolation transformer drives a receiver with the same “set-hi/set-low” data, which regenerates the original logic waveform. An internal circuit operating in the background interrogates all inputs about every 5  $\mu$ s, and in the absence of logic transitions, sends appropriate “set-hi/set-low” data across the interface. Recovery time from a fault condition or at power-up is thus between 5  $\mu$ s and 10  $\mu$ s.

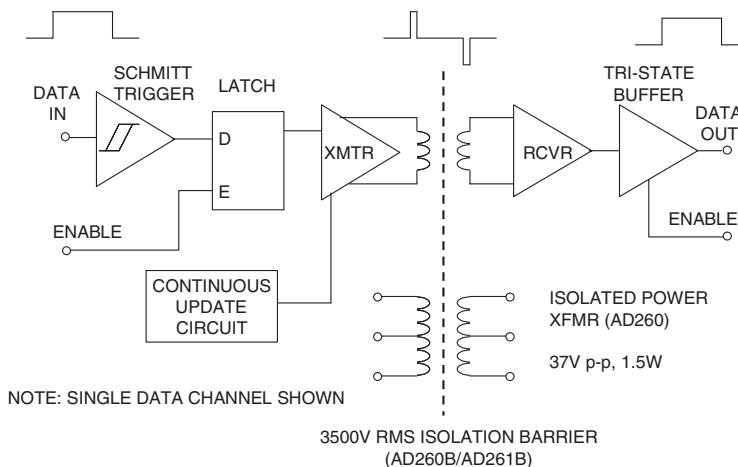


Figure 2-55: AD260/AD261 digital isolators

The power transformer (available on the AD260) is designed to operate between 150 kHz and 250 kHz and will easily deliver more than 1 W of isolated power when driven push-pull (5 V) on the transmitter side. Different transformer taps, rectifier and regulator schemes will provide combinations of  $\pm 5$  V, 15 V, 24 V, or even 30 V or higher.



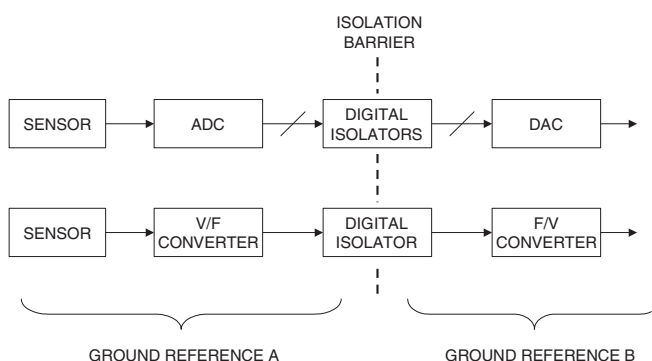
The transformer output voltage when driven with a low voltage-drop drive will be 37 V p-p across the entire secondary with a 5 V push-pull drive. Figure 2-56 summarizes the key specifications of the AD260/261 series.

- Isolation Test Voltage to 3500V rms (AD260B/AD261B)
- Five Isolated Digital Lines Available in six Input/Output Configurations
- Logic Signal Frequency: 20MHz Max.
- Data Rate: 40MBd Max.
- Isolated Power Transformer: 37V p-p, 1.5W (AD260)
- Waveform Edge Transmission Symmetry:  $\pm 1\text{ns}$
- Propagation Delay: 14ns
- Rise and Fall Times < 5ns

**Figure 2-56: AD260/AD261 digital isolator key specifications**

The availability of low cost digital isolators such as those previously discussed solves most system isolation problems in data acquisition systems as shown in Figure 2-57. In the upper example, digitizing the signal first, then using digital isolation eliminates the problem of analog isolation amplifiers. While digital isolation can be used with parallel output ADCs provided the bandwidth of the isolator is sufficient, it is more practical with ADCs that have *serial* outputs. This minimizes cost and component count. A 3-wire interface (data, serial clock, framing clock) is all that is required in these cases.

An alternative (lower example) is to use a voltage-to-frequency converter (VFC) as a transmitter and a frequency-to-voltage converter (FVC) as a receiver. In this case, only one digital isolator is required.



**Figure 2-57: Practical application of digital isolation in data acquisition systems**

## **References: Isolation Amplifiers**

1. James Conant, "Precision Wideband Three-Port Isolation Amplifier," **Analog Dialogue**, Vol. 20, No. 2, 1986, p. 14.
2. Data sheet for **AD210 Precision, Wide Bandwidth 3-Port Isolation Amplifier**, [www.analog.com](http://www.analog.com).
3. Data sheet for **AD215 120 kHz Bandwidth, Low Distortion, Isolation Amplifier**, [www.analog.com](http://www.analog.com).
4. Data sheets for **AD260 and AD261 High Speed Logic Isolators**, [www.analog.com](http://www.analog.com).
5. Chapters 2, 3, 8, Walt Kester, Editor, **Practical Design Techniques for Sensor Signal Conditioning**, Analog Devices, 1999, ISBN: 0-916550-20-6.
6. Chapter 2, Walt Kester, Editor, **Linear Design Seminar**, Analog Devices, 1995, ISBN: 0-916550-15-X.
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## CHAPTER 3

# *Using Op Amps with Data Converters*

- Section 3-1: Introduction
- Section 3-2: ADC/DAC Specifications
- Section 3-3: Driving ADC Inputs
- Section 3-4: Driving ADC/DAC Reference Outputs
- Section 3-5: Buffering DAC Outputs

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# Using Op Amps with Data Converters

Walt Kester, James Bryant, Paul Hendriks

## SECTION 3-1

### Introduction

Walt Kester

This chapter of the book deals with data conversion and associated signal conditioning circuitry involving the use of op amps. Data conversion is a very broad topic, and this chapter will provide only enough background material for the reader to make intelligent decisions regarding op amp selection. Much more material on the subject is available in the references (see References 1-5).

Figure 3-1 shows a generalized sampled data system and some possible applications of op amps. The analog input signal is first buffered and filtered before it is applied to the analog-to-digital converter (ADC). The buffer may or may not be required, depending upon the input structure of the ADC. For example, some ADCs (such as switched capacitor) generate transient currents at their inputs due to the internal conversion architecture, and these currents must be isolated from the signal source. A suitable buffer amplifier provides a low impedance drive and absorbs these currents. In some cases, an op amp is required to provide the appropriate gain and offset to match the signal to the input range of the ADC.

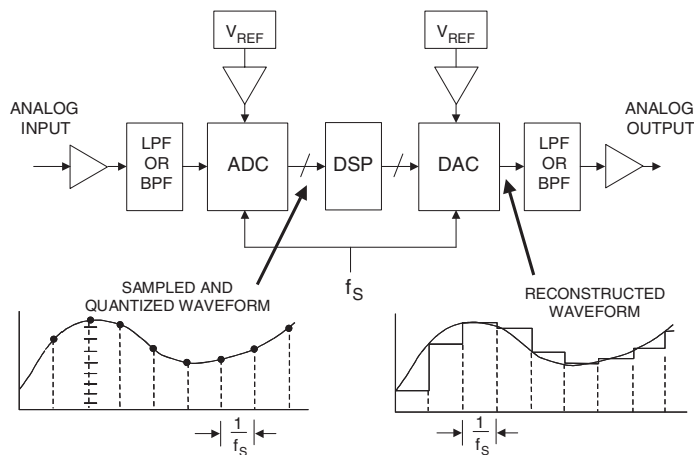


Figure 3-1: Typical sampled data system showing potential amplifier applications

Another key component in a sampled data system is the antialiasing filter which removes signals that fall outside the Nyquist bandwidth,  $f_s/2$ . Normally this filter is a low-pass filter, but it can be a band-pass filter in certain undersampling applications. If the op amp buffer is required, it may be located before or after the filter, depending on system considerations. In fact, the filter itself may be an active one, in which case the buffering function can be performed by the actual output amplifier of the filter. More discussions regarding active filters can be found in Chapter 5 of this book.

After the signal is buffered and filtered, it is applied to the ADC. The full-scale input voltage range of the ADC is generally determined by a voltage reference,  $V_{REF}$ . Some ADCs have this function on chip, while others require an external reference. If an external reference is required, its output may require buffering using an appropriate op amp. The reference input to the ADC may be connected to an internal switched capacitor network, causing transient currents to be generated at that node (similar to the analog input of such converters). Some references may therefore require a buffer to isolate these transient currents from the actual reference output. Other references may have internal buffers that are sufficient, and no additional buffering is needed in those cases.

The output of the ADC is then processed digitally by an appropriate processor, shown in the diagram as a digital signal processor (DSP). DSPs are processors that are optimized to perform fast repetitive arithmetic, as required in digital filters or fast Fourier transform (FFT) algorithms. The DSP output then drives a digital-to-analog converter (DAC) which converts the digital signal back into an analog signal.

- Gain setting
- Level-shifting
- Buffering ADC transients from signal source
- Buffering voltage reference outputs
- Buffering DAC outputs
- Active antialiasing filter before ADC
- Active anti-imaging filter after DAC

**Figure 3-2: Data converter amplifier applications**

The DAC analog output must be filtered to remove the unwanted image frequencies caused by the sampling process, and further buffering may be required to provide the proper signal amplitude and offset. The output filter is generally placed between the DAC and the buffer amplifier, but their positions can be reversed in certain applications. It is also possible to combine the filtering and buffering function if an active filter is used to condition the DAC output.

### ***Trends in Data Converters***

It is useful to examine a few general trends in data converters, to better understand any associated op amp requirements. Converter performance is first and foremost; maintaining that performance in a system application is extremely important. In low frequency measurement applications (10 Hz bandwidth signals or lower), sigma-delta ADCs with resolutions up to 24 bits are now quite common. These converters generally have automatic or factory calibration features to maintain required gain and offset accuracy. In higher frequency signal processing, ADCs must have wide dynamic range (low distortion and noise), high sampling frequencies, and generally excellent ac specifications.

In addition to sheer performance, other characteristics such as low power, single-supply operation, low cost, and small surface-mount packages also drive the data conversion market. These requirements result in

application problems because of reduced signal swings, increased sensitivity to noise, and so forth. In addition, many data converters are now produced on low-cost foundry CMOS processes which generally make on-chip amplifier design more difficult and therefore less likely to be incorporated on-chip.

As has been mentioned previously, the analog input to a CMOS ADC is usually connected directly to a switched-capacitor sample-and-hold (SHA), which generates transient currents that must be buffered from the signal source. On the other hand, data converters fabricated on Bi-CMOS or bipolar processes are more likely to have internal buffering, but generally have higher cost and power than their CMOS counterparts.

It should be clear by now that selecting an appropriate op amp for a data converter application is highly dependent on the particular converter under consideration. Generalizations are difficult, but some meaningful guidelines can be followed.

- Higher sampling rates, higher resolution, higher ac performance
- Single supply operation (e.g., 5V, 3V)
- Lower power
- Smaller input/output signal swings
- Maximize usage of low cost foundry CMOS processes
- Smaller packages
- Surface-mount technology

**Figure 3-3: Some general trends in data converters**

The most obvious requirement for a data converter buffer amplifier is that it not degrade the dc or ac performance of the converter. One might assume that a careful reading of the op amp datasheets would assist in the selection process: simply lay the data converter and the op amp datasheets side by side, and compare each critical performance specification. It is true that this method will provide some degree of success; however, in order to perform an accurate comparison, the op amp must be specified under the exact operating conditions required by the data converter application. Such factors as gain, gain setting resistor values, source impedance, output load, input and output signal amplitude, input and output common-mode (CM) level, power supply voltage, and so forth, all affect op amp performance.

It is highly unlikely that even a well written op amp data sheet will provide an exact match to the operating conditions required in the data converter application. Extrapolation of specified performance to fit the exact operating conditions can give erroneous results. Also, the op amp may be subjected to transient currents from the data converter, and the corresponding effects on op amp performance are rarely found on datasheets.

Converter datasheets themselves can be a good source for recommended op amps and other application circuits. However this information can become obsolete as newer op amps are introduced after the converter's initial release.



Analog Devices and other op amp manufacturers today have on-line websites featuring parametric search engines, which facilitate part selection (see Reference 1). For instance, the first search might be for minimum power supply voltage, e.g., 3 V. The next search might be for bandwidth, and further searches on relevant specifications will narrow the selection of op amps even further. Figure 3-4 summarizes the selection process.

- The amplifier should not degrade the performance of the ADC/DAC
- Ac specifications are usually the most important
  - Noise
  - Bandwidth
  - Distortion
- Selection based on op amp data sheet specifications difficult due to varying conditions in actual application circuit with ADC/DAC:
  - Power supply voltage
  - Signal range (differential and common-mode)
  - Loading (static and dynamic)
  - Gain
- Parametric search engines may be useful
- ADC/DAC data sheets often recommend op amps (but may not include newly released products)

**Figure 3-4: General amplifier selection criteria**

While not necessarily suitable for the final selection, this process can narrow the search to a manageable number of op amps whose individual datasheets can be retrieved, then reviewed in detail before final selection.

From the discussion thus far, it should be obvious that in order to design a proper interface, an understanding of both op amps and data converters is required. References 2-6 provide background material on data converters.

The next section of this chapter addresses key data converter performance specifications without going into the detailed operation of converters themselves. The remainder of the chapter shows a number of specific applications of op amps with various data converters.

## **References: Introduction**

1. ADI Web site, at [www.analog.com](http://www.analog.com).
2. Walt Kester, Editor, **Practical Analog Design Techniques**, Analog Devices, 1995, ISBN: 0-916550-16-8.
3. Walt Kester, Editor, **High Speed Design Techniques**, Analog Devices, 1996, ISBN: 0-916550-17-6.
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5. Chapters 2, 3, 4, Walt Kester, Editor, **Mixed-Signal and DSP Design Techniques**, Analog Devices, 2000, ISBN: 0-916550-23-0.
6. Chapters 4, 5, Walt Kester, Editor, **Linear Design Seminar**, Analog Devices, 1995, ISBN: 0-916550-15-X.

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# ADC/DAC Specifications

Walt Kester

## ADC and DAC Static Transfer Functions and DC Errors

The most important thing to remember about both DACs and ADCs is that either the input or output is digital, and therefore the signal is *quantized*. That is, an N-bit word represents one of  $2^N$  possible states, and therefore an N-bit DAC (with a fixed reference) can have only  $2^N$  possible analog outputs, and an N-bit ADC can have only  $2^N$  possible digital outputs. The analog signals will generally be voltages or currents.

The resolution of data converters may be expressed in several different ways: the weight of the Least Significant Bit (LSB), parts per million of full scale (ppm FS), millivolts (mV), and so forth. It is common that different devices (even from the same manufacturer) will be specified differently, so converter users must learn to translate between the different types of specifications if they are to successfully compare devices. The size of the least significant bit for various resolutions is shown in Figure 3-5.

RESOLUTION N	$2^N$	VOLTAGE (10V FS)	ppm FS	% FS	dB FS
2-bit	4	2.5 V	250,000	25	-12
4-bit	16	625 mV	62,500	6.25	-24
6-bit	64	156 mV	15,625	1.56	-36
8-bit	256	39.1 mV	3,906	0.39	-48
10-bit	1,024	9.77 mV (10 mV)	977	0.098	-60
12-bit	4,096	2.44 mV	244	0.024	-72
14-bit	16,384	610 $\mu$ V	61	0.0061	-84
16-bit	65,536	153 $\mu$ V	15	0.0015	-96
18-bit	262,144	38 $\mu$ V	4	0.0004	-108
20-bit	1,048,576	9.54 $\mu$ V (10 $\mu$ V)	1	0.0001	-120
22-bit	4,194,304	2.38 $\mu$ V	0.24	0.000024	-132
24-bit	16,777,216	596 nV*	0.06	0.000006	-144

\*600nV is the Johnson Noise in a 10kHz BW of a 2.2k $\Omega$  Resistor @ 25°C

Note: 10 bits and 10V FS yields an LSB of 10mV, 1000ppm, or 0.1%.  
All other values may be calculated by powers of 2.

**Figure 3-5: Quantization: the size of a least significant bit (LSB)**

As noted above (and obvious from this table), the LSB scaling for a given converter resolution can be expressed in various ways. While it is convenient to relate this to a full scale of 10 V, as in Figure 3-5, other full scale levels can be easily extrapolated.

Before we can consider op amp applications with data converters, it is necessary to consider the performance to be expected, and the specifications that are important when operating with data converters. The following sections will consider the definition of errors and specifications used for data converters.

The first applications of data converters were in measurement and control, where the exact timing of the conversion was usually unimportant, and the data rate was slow. In such applications, the dc specifications of converters are important, but timing and ac specifications are not. Today many, if not most, converters are used in *sampling* and *reconstruction* systems where ac specifications are critical (and dc ones may not be).

Figure 3-6 shows the transfer characteristics for a 3-bit unipolar ideal and nonideal DAC. In a DAC, both the input and output are quantized, and the graph consists of eight points—while it is reasonable to discuss a line through these points, it is critical to remember that the actual transfer characteristic is *not* a line, but a series of discrete points.

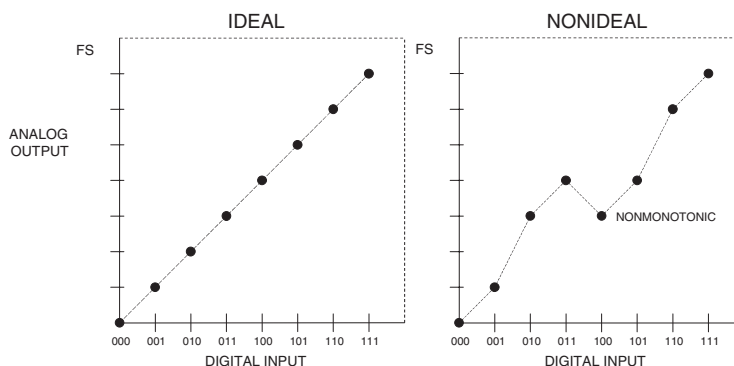


Figure 3-6: DAC transfer functions

Similarly, Figure 3-7 shows the transfer characteristics for a 3-bit unipolar ideal and nonideal ADC. Note that the input to an ADC is analog and is therefore *not* quantized, but its output *is* quantized.

The ADC transfer characteristic therefore consists of eight horizontal steps (when considering the offset, gain and linearity of an ADC we consider the line joining the midpoints of these steps).

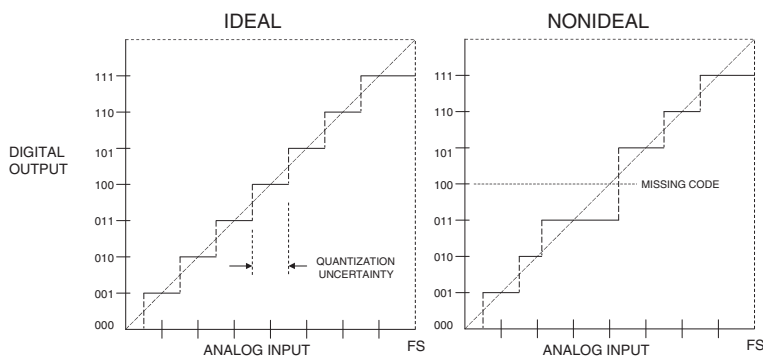


Figure 3-7: ADC transfer functions

The (ideal) ADC transitions take place at  $\frac{1}{2}$  LSB above zero, and thereafter every LSB, until  $1\frac{1}{2}$  LSB below analog full scale. Since the analog input to an ADC can take any value, but the digital output is quantized, there may be a difference of up to  $\frac{1}{2}$  LSB between the actual analog input and the exact value of the digital output. This is known as the quantization error or quantization uncertainty as shown in Figure 3-7. In ac (sampling) applications this quantization error gives rise to quantization noise which will be discussed shortly.

The *integral linearity* error of a converter is analogous to the linearity error of an amplifier, and is defined as the maximum deviation of the actual transfer characteristic of the converter from a straight line. It is generally expressed as a percentage of full scale (but may be given in LSBs). There are two common ways of choosing the straight line: *end point* and *best straight line*.

In the end point system, the deviation is measured from the straight line through the origin and the full scale point (after gain adjustment). This is the most useful integral linearity measurement for measurement and control applications of data converters (since error budgets depend on deviation from the ideal transfer characteristic, not from some arbitrary “best fit”), and is the one normally adopted by Analog Devices, Inc.

The best straight line, however, does give a better prediction of distortion in ac applications, and also gives a lower value of “linearity error” on a data sheet. The best fit straight line is drawn through the transfer characteristic of the device using standard curve fitting techniques, and the maximum deviation is measured from this line. In general, the integral linearity error measured in this way is only 50% of the value measured by end point methods. This makes the method good for producing impressive datasheets, but it is less useful for error budget analysis. For ac applications, it is even better to specify distortion than dc linearity, so it is rarely necessary to use the best straight line method to define converter linearity.

The other type of converter nonlinearity is *differential nonlinearity* (DNL). This relates to the linearity of the code transitions of the converter. In the ideal case, a change of 1 LSB in digital code corresponds to a change of exactly 1 LSB of analog signal. In a DAC, a change of 1 LSB in digital code produces exactly 1 LSB change of analog output, while in an ADC there should be exactly 1 LSB change of analog input to move from one digital transition to the next.

Where the change in analog signal corresponding to 1 LSB digital change is more or less than 1 LSB, there is said to be a DNL error. The DNL error of a converter is normally defined as the maximum value of DNL to be found at any transition.

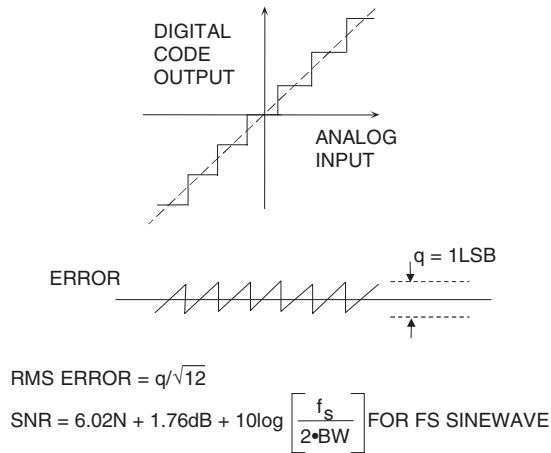
If the DNL of a DAC is less than  $-1$  LSB at any transition (Figure 3-6), the DAC is *nonmonotonic*; i.e., its transfer characteristic contains one or more localized maxima or minima. A DNL greater than  $+1$  LSB does not cause nonmonotonicity, but is still undesirable. In many DAC applications (especially closed-loop systems where nonmonotonicity can change negative feedback to positive feedback), it is critically important that DACs are monotonic. DAC monotonicity is often explicitly specified on datasheets, but if the DNL is guaranteed to be less than 1 LSB (i.e.,  $|DNL| \leq 1\text{LSB}$ ) then the device must be monotonic, even without an explicit guarantee.

ADCs can be nonmonotonic, but a more common result of excess DNL in ADCs is *missing codes* (Figure 3-7). Missing codes (or nonmonotonicity) in an ADC are as objectionable as nonmonotonicity in a DAC. Again, they result from  $DNL > 1\text{LSB}$ .

## Quantization Noise in Data Converters

The only errors (dc or ac) associated with an ideal N-bit ADC are those related to the sampling and quantization processes. The maximum error an ideal ADC makes when digitizing a dc input signal is  $\pm\frac{1}{2}$  LSB. Any ac signal applied to an ideal N-bit ADC will produce quantization noise whose rms value (measured over the Nyquist bandwidth, dc to  $f_s/2$ ) is approximately equal to the weight of the least significant bit (LSB), q,

divided by  $\sqrt{12}$ . This assumes that the signal is at least a few LSBs in amplitude so that the ADC output always changes state. The quantization error signal from a linear ramp input is approximated as a sawtooth waveform with a peak-to-peak amplitude equal to  $q$ , and its rms value is therefore  $q/\sqrt{12}$  (see Figure 3-8).



**Figure 3-8: Ideal N-bit ADC quantization noise**

It can be shown that the ratio of the rms value of a full scale sinewave to the rms value of the quantization noise (expressed in dB) is:

$$\text{SNR} = 6.02N + 1.76\text{dB}, \quad \text{Eq. 3-1}$$

where  $N$  is the number of bits in the ideal ADC. *Note—this equation is only valid if the noise is measured over the entire Nyquist bandwidth from dc to  $f_s/2$ .* If the signal bandwidth,  $\text{BW}$ , is less than  $f_s/2$ , the SNR within the signal bandwidth  $\text{BW}$  is increased because the amount of quantization noise within the signal bandwidth is less.

The correct expression for this condition is given by:

$$\text{SNR} = 6.02N + 1.76\text{ dB} + 10\log\left(\frac{f_s}{2 \cdot \text{BW}}\right). \quad \text{Eq. 3-2}$$

The above equation reflects the condition called *oversampling*, where the sampling frequency is higher than twice the signal bandwidth. The correction term is often called *processing gain*. Notice that for a given signal bandwidth, doubling the sampling frequency increases the SNR by 3 dB.

## ADC Input-Referred Noise

The internal circuits of an ADC produce a certain amount of wideband rms noise due to thermal and  $kT/C$  effects. This noise is present even for dc input signals, and accounts for the fact that the output of most wideband (or high resolution) ADCs is a distribution of codes, centered around the nominal dc input value, as is shown in Figure 3-9.

To measure its value, the input of the ADC is grounded, and a large number of output samples are collected and plotted as a histogram (sometimes referred to as a *grounded-input* histogram).

Since the noise is approximately Gaussian, the standard deviation ( $\sigma$ ) of the histogram is easily calculated, corresponding to the effective input rms noise. It is common practice to express this rms noise in terms of LSBs, although it can be expressed as an rms voltage.

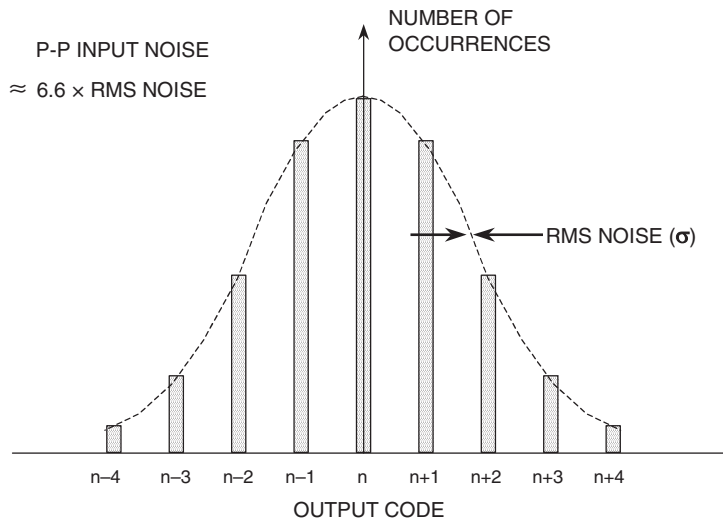


Figure 3-9: Effect of ADC input-referred noise on “grounded input” histogram



## Calculating Op Amp Output Noise and Comparing it with ADC Input-Referred Noise

In precision measurement applications utilizing 16- to 24-bit sigma-delta ADCs operating on low frequency (<20 Hz, e.g.) signals, it is generally undesirable to use a drive amplifier in front of the ADC because of the increased noise due to the amplifier itself. If an op amp is required, however, the op amp output 1/f noise should be compared to the input-referred ADC noise. The 1/f noise is usually specified as a peak-to-peak value measured over the 0.1 Hz to 10 Hz bandwidth and referred to the op amp input (see Chapter 1 of this book). Op amps such as the OP177 and the AD707 (input voltage noise 350 nV p-p) or the AD797 (input voltage noise 50 nV p-p) are appropriate for high resolution measurement applications if required.

The general model for calculating the referred-to-input (RTI) or referred-to-output (RTO) noise of an op amp is shown in Figure 3-10. This model shows all possible noise sources. The results using this model are relatively accurate, provided there is less than 1 dB gain peaking in the closed loop frequency response. For higher frequency applications, 1/f noise can be neglected, because the dominant contributor is white noise.

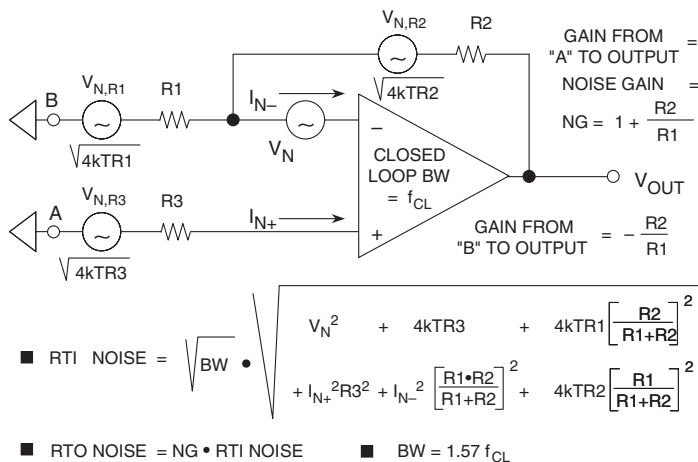
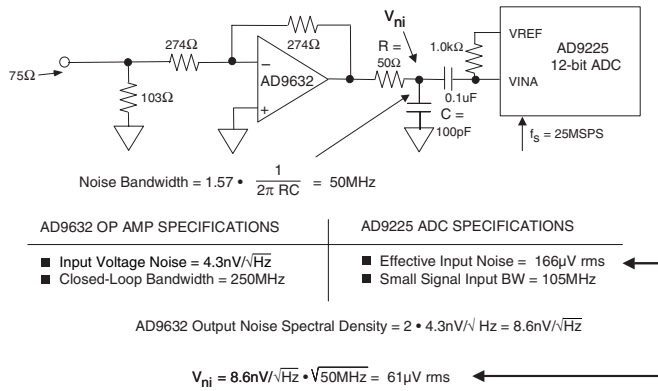


Figure 3-10: Op amp noise model for a first-order circuit with resistive feedback

An example of a practical noise calculation is shown in Figure 3-11. In this circuit, a wideband, low distortion amplifier (AD9632) drives a 12-bit, 25 MSPS ADC (AD9225). The input voltage noise spectral density of the AD9632 ( $4.3 \text{ nV} / \sqrt{\text{Hz}}$ ) dominates the op amp noise because of the low gain and the low values of the external feedback resistors. The noise at the output of the AD9632 is obtained by multiplying the input voltage noise spectral density by the noise gain of 2. To obtain the rms noise, the noise spectral density is multiplied by the equivalent noise bandwidth of 50 MHz which is set by the single-pole low-pass filter placed between the op amp and the ADC input.

Note that the closed-loop bandwidth of the AD9632 is 250 MHz, and the input bandwidth of the AD9225 is 105 MHz. With no filter, the output noise of the AD9632 would be integrated over the full 105 MHz ADC input bandwidth.

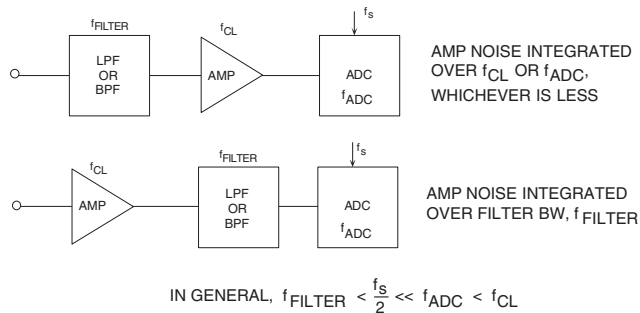
However, the sampling frequency of the ADC is 25 MSPS, thereby implying that signals above 12.5 MHz are not of interest, assuming Nyquist operation (as opposed to undersampling applications where the input signal can be greater than the Nyquist frequency,  $f_s/2$ ). The addition of this simple filter significantly reduces noise effects.



**Figure 3-11: Noise calculations for the AD9632 op amp driving the AD9225 12-bit, 25 MSPS ADC**

The noise at the output of the low-pass filter is calculated as approximately 61 μV rms which is less than half the effective input noise of the AD9225, 166 μV rms. Without the filter, the noise from the op amp would be about 110 μV rms (integrating over the full equivalent ADC input noise bandwidth of  $1.57 \times 105 \text{ MHz} = 165 \text{ MHz}$ ).

This serves to illustrate the general concept shown in Figure 3-12. In most high speed system applications a passive antialiasing filter (either low-pass for baseband sampling, or band-pass for undersampling) is required, and placing this filter between the op amp and the ADC will serve to reduce the noise due to the op amp.



**Figure 3-12: Proper positioning of the antialiasing filter will reduce the effects of op amp noise**

## Quantifying and Measuring Converter Dynamic Performance

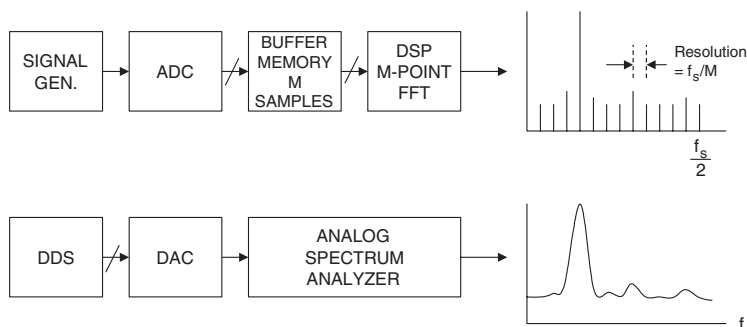
There are various ways to characterize the ac performance of ADCs. In the early years of ADC technology (over 30 years ago) there was little standardization with respect to ac specifications, and measurement equipment and techniques were not well understood or available. Over nearly a 30-year period, manufacturers and customers have learned more about measuring the dynamic performance of converters, and the specifications shown in Figure 3-13 represent the most popular ones used today.

- Signal-to-Noise-and-Distortion Ratio (SINAD, or S/N + D)
- Effective Number of Bits (ENOB)
- Signal-to-Noise Ratio (SNR)
- Analog Bandwidth (Full-Power, Small-Signal)
- Harmonic Distortion
- Worst Harmonic
- Total Harmonic Distortion (THD)
- Total Harmonic Distortion Plus Noise (THD + N)
- Spurious Free Dynamic Range (SFDR)
- Two-Tone Intermodulation Distortion
- Multitone Intermodulation Distortion

**Figure 3-13: Quantifying ADC dynamic performance**

Practically all the specifications represent the converter's performance in the frequency domain, and all are related to noise and distortion in one manner or another.

ADC outputs are analyzed using fast Fourier transform (FFT) techniques, and DAC outputs are analyzed using conventional analog spectrum analyzers, as shown in Figure 3-14. In the case of an ADC, the input signal is an analog sinewave, and in the case of a DAC, the input is a digital sinewave generated by a direct digital synthesis (DDS) system.



**Figure 3-14: Measuring ADC/DAC dynamic performance**

## Signal-to-Noise-and-Distortion Ratio (SINAD), Signal-to-Noise Ratio (SNR), and Effective Number of Bits (ENOB)

SINAD and SNR deserve careful attention (see Figure 3-15), because there is still some variation between ADC manufacturers as to their precise meaning. *Signal-to-noise-and-Distortion* (SINAD, or S/N+D) is the ratio of the rms signal amplitude to the mean value of the root-sum-square (RSS) of all other spectral components, *including harmonics*, but excluding dc. SINAD is a good indication of the overall dynamic performance of an ADC as a function of input frequency, because it includes all components that make up noise (including thermal noise) and distortion. It is often plotted for various input amplitudes. SINAD is equal to THD+N if the bandwidth for the noise measurement is the same.

- SINAD (Signal-to-Noise-and-Distortion Ratio):
  - The ratio of the rms signal amplitude to the mean value of the root-sum-squares (RSS) of all other spectral components, including harmonics, but excluding dc.

- ENOB (Effective Number of Bits):

$$\text{ENOB} = \frac{\text{SINAD} - 1.76 \text{ dB}}{6.02}$$

- SNR (Signal-to-Noise Ratio, or Signal-to-Noise Ratio without Harmonics):
  - The ratio of the rms signal amplitude to the mean value of the root-sum-squares (RSS) of all other spectral components, excluding the first five harmonics and dc.

**Figure 3-15: SINAD, ENOB, and SNR**

The SINAD plot shows where the ac performance of the ADC degrades due to high-frequency distortion, and is usually plotted for frequencies well above the Nyquist frequency so that performance in undersampling applications can be evaluated.

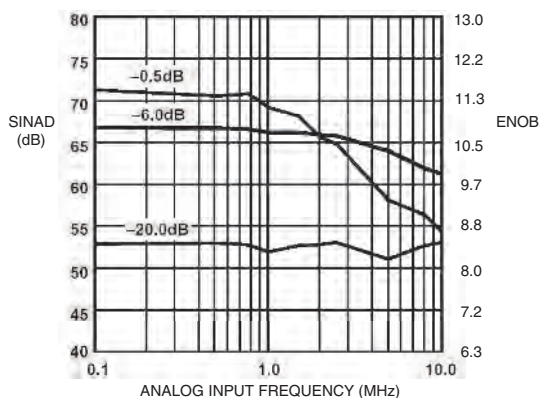
SINAD is often converted to *effective-number-of-bits* (ENOB) using the relationship for the theoretical SNR of an ideal N-bit ADC:  $\text{SNR} = 6.02N + 1.76\text{dB}$ . The equation is solved for N, and the value of SINAD is substituted for SNR:

$$\text{ENOB} = \frac{\text{SINAD} - 1.76 \text{ dB}}{6.02} \quad \text{Eq. 3-3}$$

*Signal-to-noise ratio* (SNR, or *SNR-without-harmonics*) is calculated the same as SINAD except that the signal harmonics are excluded from the calculation, leaving only the noise terms. In practice, it is only necessary to exclude the first five harmonics since they dominate. The SNR plot will degrade at high frequencies, but not as rapidly as SINAD because of the exclusion of the harmonic terms.

Many current ADC datasheets somewhat loosely refer to SINAD as SNR, so the design engineer must be careful when interpreting these specifications.

A SINAD/ENOB plot for the AD9220 12-bit, 10MSPS ADC is shown in Figure 3-16.

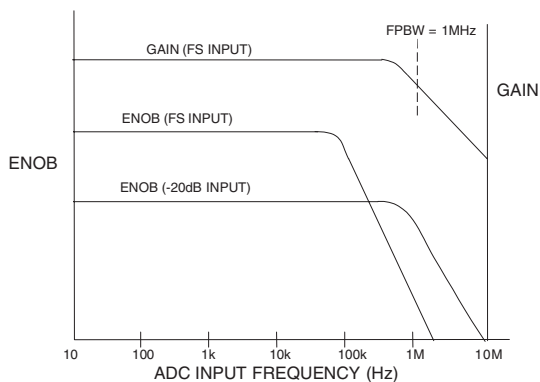


**Figure 3-16: AD9220 12-bit, 10 MSPS ADC SINAD and ENOB for various input signal levels**

### Analog Bandwidth

The analog bandwidth of an ADC is that frequency at which the spectral output of the *fundamental* swept frequency (as determined by the FFT analysis) is reduced by 3 dB. It may be specified for either a small signal bandwidth (SSBW), or a full-scale signal (FPBW – full power bandwidth), so there can be a wide variation in specifications between manufacturers.

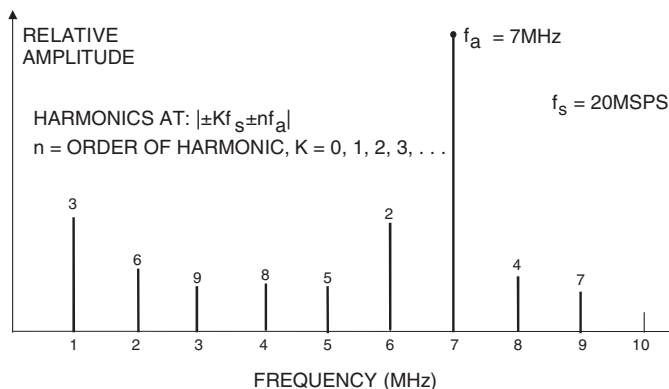
Like an amplifier, the analog bandwidth specification of a converter does not imply that the ADC maintains good distortion performance up to its bandwidth frequency. In fact, the SINAD (or ENOB) of most ADCs will begin to degrade considerably before the input frequency approaches the actual 3 dB bandwidth frequency. Figure 3-17 shows ENOB and full-scale frequency response of an ADC with a FPBW of 1 MHz; however, the ENOB begins to drop rapidly above 100 kHz.



**Figure 3-17: ADC Gain (bandwidth) and ENOB versus frequency shows importance of ENOB specification**

## Harmonic Distortion, Worst Harmonic, Total Harmonic Distortion (THD), Total Harmonic Distortion Plus Noise (THD + N)

There are a number of ways to quantify the distortion of an ADC. An FFT analysis can be used to measure the amplitude of the various harmonics of a signal. The harmonics of the input signal can be distinguished from other distortion products by their location in the frequency spectrum. Figure 3-18 shows a 7 MHz input signal sampled at 20 MSPS and the location of the first nine harmonics.



**Figure 3-18: Location of harmonic distortion products:**  
Input signal = 7 MHz, sampling rate = 20 MSPS

Aliased harmonics of  $f_a$  fall at frequencies equal to  $|\pm K f_s \pm n f_a|$ , where  $n$  is the order of the harmonic, and  $K = 0, 1, 2, 3, \dots$ . The second and third harmonics are generally the only ones specified on a data sheet because they tend to be the largest, although some datasheets may specify the value of the *worst* harmonic.

*Harmonic distortion* is normally specified in dBc (decibels below *carrier*), although in audio applications it may be specified as a percentage. Harmonic distortion is generally specified with an input signal near full scale (generally 0.5 dB to 1 dB below full scale to avoid clipping), but it can be specified at any level. For signals much lower than full scale, other distortion products due to the DNL of the converter (not direct harmonics) may limit performance.

*Total harmonic distortion* (THD) is the ratio of the rms value of the fundamental signal to the mean value of the root-sum-square of its harmonics (generally, only the first five are significant). THD of an ADC is also generally specified with the input signal close to full scale, although it can be specified at any level.

*Total harmonic distortion plus noise* (THD + N) is the ratio of the rms value of the fundamental signal to the mean value of the root-sum-square of its harmonics plus all noise components (excluding dc). The bandwidth over which the noise is measured must be specified. In the case of an FFT, the bandwidth is dc to  $f_s/2$ . (If the bandwidth of the measurement is dc to  $f_s/2$ , THD + N is equal to SINAD.)

## Spurious Free Dynamic Range (SFDR)

Probably the most significant specification for an ADC used in a communications application is its spurious free dynamic range (SFDR). The SFDR specification is to ADCs what the third order intercept specification is to mixers and LNAs.

SFDR of an ADC is defined as the ratio of the rms signal amplitude to the rms value of the *peak spurious spectral content* (measured over the entire first Nyquist zone, dc to  $f_s/2$ ). SFDR is generally plotted as a function of signal amplitude and may be expressed relative to the signal amplitude (dBc) or the ADC full scale (dBFS) as shown in Figure 3-19.

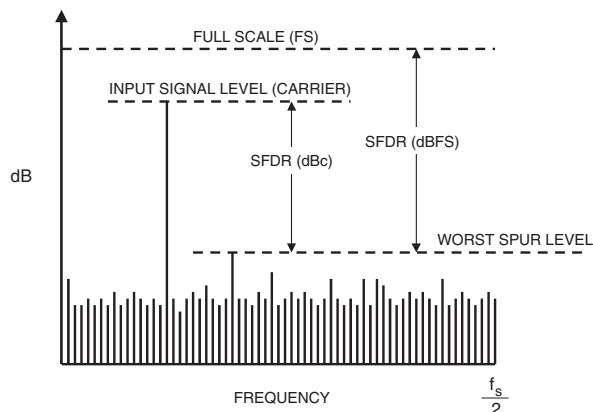


Figure 3-19: Spurious free dynamic range (SFDR)

For a signal near full scale, the peak spectral spur is generally determined by one of the first few harmonics of the fundamental. However, as the signal falls several dB below full scale, other spurs generally occur which are not direct harmonics of the input signal. This is because of the differential nonlinearity of the ADC transfer function as discussed earlier. Therefore, SFDR considers *all* sources of distortion, regardless of their origin.

### Two-Tone Intermodulation Distortion (IMD)

Two-tone IMD is measured by applying two spectrally pure sinewaves to the ADC at frequencies  $f_1$  and  $f_2$ , usually relatively close together. The amplitude of each tone is set slightly more than 6 dB below full scale so that the ADC does not clip when the two tones add in-phase. Second- and third-order product locations are shown in Figure 3-20.

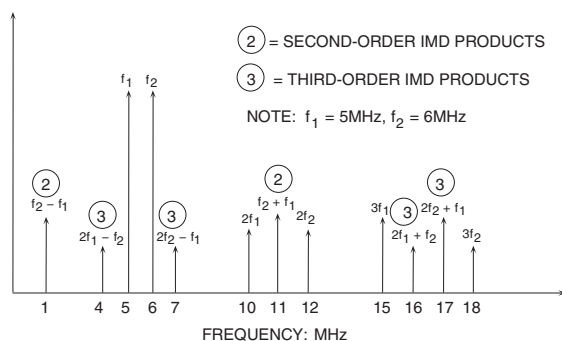


Figure 3-20: Second and third-order intermodulation products for  $f_1 = 5$  MHz,  $f_2 = 6$  MHz

Notice that the second-order products fall at frequencies which can be removed by digital filters. However, the third-order products  $2f_2 - f_1$  and  $2f_1 - f_2$  are close to the original signals, and are almost impossible to filter. Unless otherwise specified, two-tone IMD refers to these third-order products. The value of the IMD product is expressed in dBc relative to the value of *either* of the two original tones, and not to their sum.

Note, however, that if the two tones are close to  $f_s/4$ , the aliased third harmonics of the fundamentals can make the identification of the actual  $2f_2 - f_1$  and  $2f_1 - f_2$  products difficult. This is because the third harmonic of  $f_s/4$  is  $3f_s/4$ , and the alias occurs at  $f_s - 3f_s/4 = f_s/4$ . Similarly, if the two tones are close to  $f_s/3$ , the aliased second harmonics may interfere with the measurement. The same reasoning applies here; the second harmonic of  $f_s/3$  is  $2f_s/3$ , and its alias occurs at  $f_s - 2f_s/3 = f_s/3$ .

The concept of *second- and third-order intercept points* is not valid for an ADC, because the distortion products don't vary predictably (as a function of signal amplitude). The ADC doesn't gradually begin to compress signals approaching full scale (there is no 1 dB compression point); it acts as a *hard limiter* as soon as the signal exceeds the input range, producing extreme distortion due to clipping. Conversely, for signals much below full scale, the distortion floor remains relatively constant and is independent of signal level.

Multitone SFDR is often measured in communications applications. The larger number of tones more closely simulates the wideband frequency spectrum of cellular telephone systems such as AMPS or GSM. High SFDR increases the receiver's ability to capture small signals in the presence of large ones, and prevent the small signals from being masked by the intermodulation products of the larger ones.



**References: ADC/DAC Specifications**

1. Walt Kester, Editor, **Practical Analog Design Techniques**, Analog Devices, 1995, ISBN: 0-916550-16-8.
2. Walt Kester, Editor, **High Speed Design Techniques**, Analog Devices, 1996, ISBN: 0-916550-17-6.
3. Chapters 3, 8, Walt Kester, Editor, **Practical Design Techniques for Sensor Signal Conditioning**, Analog Devices, 1999, ISBN: 0-916550-20-6.
4. Chapters 2, 3, 4, Walt Kester, Editor, **Mixed-Signal and DSP Design Techniques**, Analog Devices, 2000, ISBN: 0-916550-23-0.
5. Chapters 4, 5, Walt Kester, Editor, **Linear Design Seminar**, Analog Devices, 1995, ISBN: 0-916550-15-X.

## Driving ADC Inputs

Walt Kester, Paul Hendriks

### Introduction

Op amps are often used as drivers for ADCs to provide the gain and level-shifting required for the input signal to match the input range of the ADC. An op amp may be required because of the antialiasing filter impedance matching requirements. In some cases, the antialiasing filter may be an active filter and include op amps as part of the filter itself. Some ADCs also generate transient currents on their inputs due to the conversion process, and these must be isolated from the signal source with an op amp. This section examines these and other issues involved in driving high performance ADCs.

To begin with, one shouldn't necessarily assume that a driver op amp is always required. Some converters have relatively benign inputs and are designed to interface directly to the signal source. There is practically no industry standardization regarding ADC input structures, and therefore each ADC must be carefully examined on its own merits before designing the input interface circuitry. In some applications, transformer drive may be preferable.

Assuming an op amp is required for one reason or another, the task of its selection is a critical one and not at all straightforward. Figure 3-21 lists a few of the constraints and variables. *The most important requirement is that the op amp should not significantly degrade the overall dc or ac performance of the ADC.* At first glance, it would appear that a careful comparison of an op amp data sheet with the ADC data sheet would allow an appropriate choice. However, this is rarely the case.

- Minimize degradation of ADC/DAC performance specifications
- Fast settling to ADC/DAC transient
- High bandwidth
- Low noise
- Low distortion
- Low power
  
- Note: Op amp performance must be measured under identical conditions as encountered in ADC/DAC application
  - Gain setting resistors
  - Input source impedance, output load impedance
  - Input / output signal voltage range
  - Input signal frequency
  - Input / output common-mode level
  - Power supply voltage (single or dual supply)
  - Transient loading

**Figure 3-21: General op amp requirements in ADC driver applications**

The problem is that the op amp performance specifications must be known for the *exact* circuit configuration used in the ADC driver circuit. Even a very complete data sheet is unlikely to provide all information required, due to the wide range of possible variables.

Although the op amp and ADC datasheets should definitely be used as a guide in the selection process, it is unlikely that the overall performance of the op amp/ADC combination can be predicted accurately without actually prototyping the circuit, especially in high performance applications.

Various tested application circuits are often recommended on either the op amp or the ADC data sheet, but these can become obsolete quickly as new op amps are released. In most cases, however, the ADC data sheet application section should be used as the primary source for tested interfaces.

### ***Op Amp Specifications Key to ADC Applications***

The two most popular applications for ADCs today are in either precision high-resolution measurements or in low distortion high speed systems. Precision measurement applications require ADCs of at least 16 bits of resolution, and sometimes up to 24 bits. Op amps used with these ADCs must be low noise and have excellent dc characteristics. In fact, high resolution measurement ADCs are often designed to interface directly with the transducer, eliminating the need for an op amp entirely.

If op amps are required, it is generally relatively straightforward to select one based on well understood dc specifications, as listed in Figure 3-22.

- Dc
  - Offset, offset drift
  - Input bias current
  - Open loop gain
  - Integral linearity
  - 1/f noise (voltage and current)
- Ac (Highly Application-Dependent)
  - Wideband noise (voltage and current)
  - Small and Large Signal Bandwidth
  - Harmonic Distortion
  - Total Harmonic Distortion (THD)
  - Total Harmonic Distortion + Noise (THD + N)
  - Spurious Free Dynamic Range (SFDR)
  - Third-Order Intermodulation Distortion
  - Third-Order Intercept Point

**Figure 3-22: Key op amp specifications**

It is much more difficult to provide a complete set of op amp ac specifications because they are highly dependent upon the application circuit. For example, Figure 3-23 shows some key specifications taken from the table of specifications on the data sheet for the AD8057/AD8058 high speed, low distortion op amp (see Reference 1). Note that the specifications depend on the supply voltage, the signal level, output loading, and so forth. It should also be emphasized that it is customary to provide only *typical* ac specifications (as opposed to *maximum* and *minimum* values) for most op amps. In addition, there are restrictions on the input and output CM signal ranges, which are especially important when operating on low voltage dual (or single) supplies.

Most op amp datasheets contain a section that provides supplemental performance data for various other conditions not explicitly specified in the primary specification tables. For instance, Figure 3-24 shows the

	$V_S = \pm 5V$	$V_S = +5V$
Input Common-Mode Voltage Range	-4.0V to +4.0V	0.9V to 3.4V
Output Common-Mode Voltage Range	-4.0V to +4.0V	0.9V to 4.1V
Input Voltage Noise	$7nV/\sqrt{Hz}$	$7nV/\sqrt{Hz}$
Small Signal Bandwidth	325MHz	300MHz
THD @ 5MHz, $V_O = 2V$ p-p, $R_L = 1k\Omega$	-85dBc	-75dBc
THD @ 20MHz, $V_O = 2V$ p-p, $R_L = 1k\Omega$	-62dBc	-54dBc

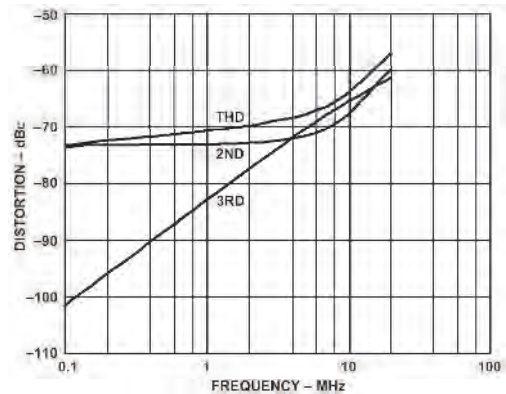
**Figure 3-23: AD8057/AD8058 op amp key ac specifications,  $G = +1$**

AD8057/AD8058 distortion as a function of frequency for  $G = +1$  and  $V_S = \pm 5V$ . Unless it is otherwise specified, the data represented by these curves should be considered typical (it is usually marked as such).

Note however that the data in both Figure 3-24 (and Figure 3-25) is given for a dc load of  $150\Omega$ . This is a load presented to the op amp in the popular application of driving a source and load-terminated  $75\Omega$  cable. Distortion performance is generally better with lighter dc loads, such as  $500\Omega - 1000\Omega$  (more typical of many ADC inputs), and this data may or may not be found on the data sheet.

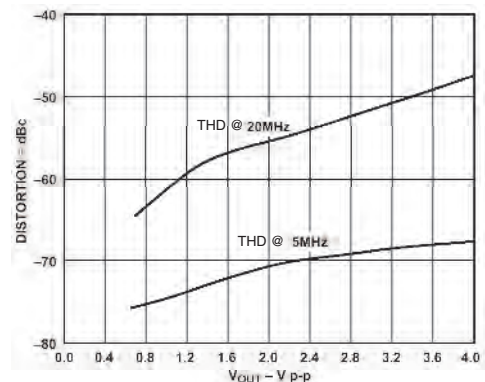
**Figure 3-24: AD8057/AD8058 op amp distortion versus frequency**

$G = +1$ ,  $R_L = 150\Omega$ ,  $V_S = \pm 5V$



**Figure 3-25: AD8057/AD8058 op amp distortion versus output voltage**

$G = +1$ ,  $R_L = 150\Omega$ ,  $V_S = \pm 5V$



On the other hand, Figure 3-25 shows distortion as a function of output signal level for a frequencies of 5 MHz and 20 MHz.

Whether or not specifications such as those just described are complete enough to select an op amp for an ADC driver application depends upon the ability to match op amp specifications to the actually required ADC operating conditions. In many cases, these comparisons will at least narrow the op amp selection process. The following sections will examine a number of specific driver circuit examples using various types of ADCs, ranging from high resolution measurement to high speed, low distortion applications.

### ***Driving High Resolution Sigma-Delta Measurement ADCs***

The AD77XX family of ADCs is optimized for high resolution (16–24 bits) low frequency transducer measurement applications. Details of operation can be found in Reference 2, and general characteristics of the family are listed in Figure 3-26.

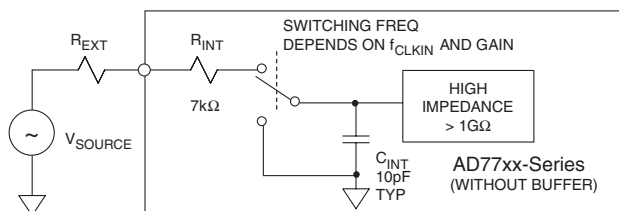
- Resolution: 16 – 24 bits
- Input signal bandwidth: <60Hz
- Effective sampling rate: <100Hz
- Generally Sigma-Delta architecture
- Designed to interface directly to sensors (< 1 k $\Omega$ ) such as bridges with no external buffer amplifier (e.g., AD77xx series)
  - On-chip PGA and high resolution ADC eliminates the need for external amplifier
- If buffer is used, it should be precision low noise (especially 1/f noise)
  - OP177
  - AD707
  - AD797

**Figure 3-26: High resolution low frequency measurement ADCs**

Some members of this family, such as the AD7730, have a high impedance input buffer which isolates the analog inputs from switching transients generated in the front end programmable gain amplifier (PGA) and the sigma-delta modulator. Therefore, no special precautions are required in driving the analog inputs. Other members of the AD77xx family, however, either do not have the input buffer or, if one is included on-chip, it can be switched either in or out under program control. Bypassing the buffer offers a slight improvement in noise performance.

The equivalent input circuit of the AD77xx family without an input buffer is shown in Figure 3-27. The input switch alternates between the 10 pF sampling capacitor and ground. The 7 k $\Omega$  internal resistance,  $R_{INT}$ , is the on resistance of the input multiplexer. The switching frequency is dependent on the frequency of the input clock and also the internal PGA gain. If the converter is working to an accuracy of 20-bits, the 10 pF internal capacitor,  $C_{INT}$ , must charge to 20-bit accuracy during the time the switch connects the capacitor to the input. This interval is one-half the period of the switching signal (it has a 50% duty cycle). The input RC time constant due to the 7 k $\Omega$  resistor and the 10 pF sampling capacitor is 70 ns. If the charge is to achieve 20-bit accuracy, the capacitor must charge for at least 14 time constants, or 980 ns. Any external resistance in series with the input will increase this time constant.

There are tables on the datasheets for the various AD77xx ADCs, which give the maximum allowable values of  $R_{EXT}$  in order to maintain a given level of accuracy. These tables should be consulted if the external source resistance is more than a few k $\Omega$ .



- $R_{EXT}$  Increases  $C_{INT}$  Charge Time and May Result in Gain Error
- Charge Time Dependent on the Input Sampling Rate and Internal PGA Gain Setting
- Refer to Specific Data Sheet for Allowable Values of  $R_{EXT}$  to Maintain Desired Accuracy
- Some AD77xx-Series ADCs Have Internal Buffering which Isolates Input from Switching Circuits

Figure 3-27: Driving unbuffered AD77xx-series  $\Sigma$ - $\Delta$  ADC inputs

Note that for instances where an external op amp buffer is found to be required with this type of converter, guidelines exist for best overall performance. This amplifier should be a precision low noise bipolar input type, such as the OP177, AD707, or the AD797.

### Op Amp Considerations for Multiplexed Data Acquisition Applications

Multiplexing is a fundamental part of many data acquisition systems. Switches used in multiplexed data acquisition systems are generally CMOS-types shown in Figure 3-28. Utilizing P-Channel and N-Channel MOSFET switches in parallel minimizes the change of *on resistance* ( $R_{ON}$ ) as a function of signal voltage. On resistance can vary from less than five to several hundred ohms, depending upon the device. Variation in on resistance as a function of signal level (often called  *$R_{ON}$ -modulation*) causes distortion if the multiplexer drives a load, therefore  *$R_{ON}$ -flatness* is also an important specification.

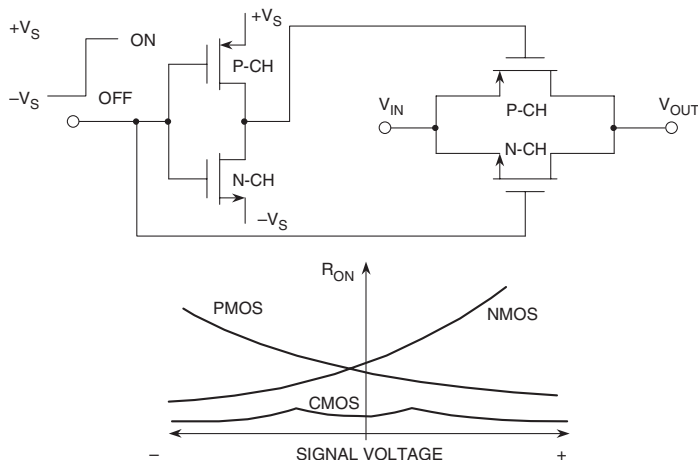
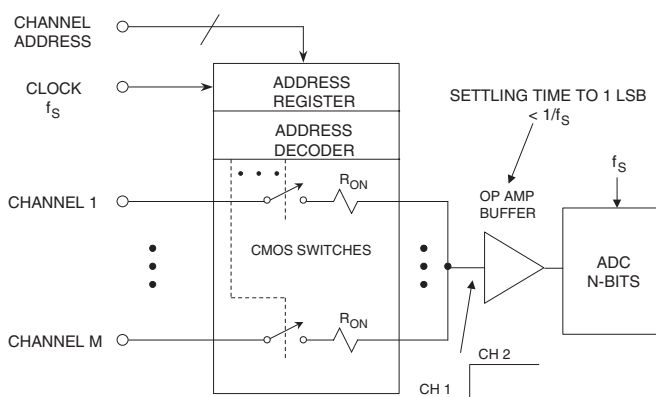


Figure 3-28: Basic CMOS analog switch

Because of the effects of nonzero  $R_{ON}$  and  $R_{ON}$ -modulation, multiplexer outputs should be isolated from the load with a suitable buffer op amp. A separate buffer is not required if the multiplexer drives a high input impedance, such as a PGA, SHA or ADC—but beware. Some SHAs and ADCs draw high frequency pulse current at their sampling rate and cannot tolerate being driven by an unbuffered multiplexer.

Key multiplexer specifications are *switching time*, *on resistance*, *on resistance flatness*, and *off-channel isolation*, and *crosstalk*. Multiplexer switching time ranges from less than 20 ns to over 1  $\mu$ s,  $R_{ON}$  from less than 5  $\Omega$  to several hundred ohms, and off-channel isolation from 50 dB to 90 dB.

A number of CMOS switches can be connected to form an analog multiplexer, as shown in Figure 3-29. The number of input channels typically ranges from 4 to 16, and some multiplexers have internal channel-address decoding logic and registers, while with others, these functions must be performed externally. Unused multiplexer inputs *must* be grounded or severe loss of system accuracy may result. In applications requiring an op amp buffer, it should be noted that when the multiplexer changes channels it is possible to have a full-scale step function into the op amp and the ADC that follows it.



**Figure 3-29: Typical multiplexed data acquisition system requires fast settling op amp buffer**

Op amp settling time must be fast enough so that conversion errors do not result. It is customary to specify the op amp settling time to 1 LSB, and the allowed time for this settling is generally the reciprocal of the sampling frequency.

### Driving Single-Supply Data Acquisition ADCs with Scaled Inputs

The AD789x and AD76xx family of single supply SAR ADCs (as well as the AD974, AD976, and AD977) includes a thin film resistive attenuator and level shifter on the analog input to allow a variety of input range options, both bipolar and unipolar.

A simplified diagram of the input circuit of the AD7890-10 12-bit, 8-channel ADC is shown in Figure 3-30. This arrangement allows the converter to digitize a  $\pm 10$  V input while operating on a single +5 V supply.

Within the ADC, the R1/R2/R3 thin film network provides attenuation and level shifting to convert the  $\pm 10$  V input to a 0 V to +2.5 V signal that is digitized. This type of input requires no special drive circuitry, because R1 isolates the input from the actual converter circuitry that may generate transient currents due to

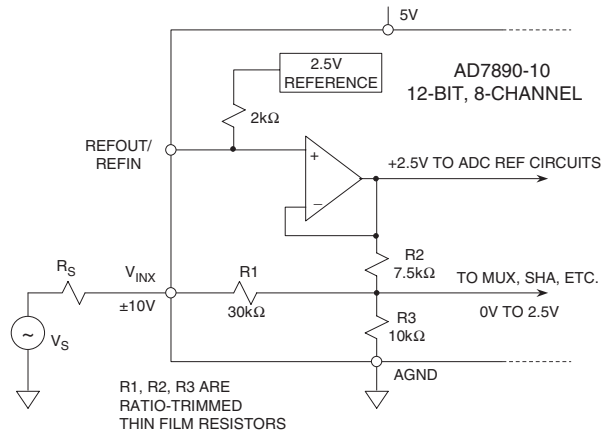


Figure 3-30: Driving single-supply data acquisition ADCs with scaled inputs

the conversion process. Nevertheless, the external source resistance  $R_S$  should be kept reasonably low, to prevent gain errors caused by the  $R_S/R_1$  divider.

### Driving ADCs with Buffered Inputs

Some ADCs have on-chip buffer amplifiers on their analog input to simplify the interface. This feature is most often found on ADCs designed on either bipolar or BiCMOS processes. Conversely, input amplifiers are rarely found on CMOS ADCs because of the inherent difficulty associated with amplifier design in CMOS.

A typical input structure for an ADC with an input buffer is shown in Figure 3-31 for the AD9042 12-bit, 41 MSPS ADC. The effective input impedance is 250  $\Omega$ , and an external 61.9  $\Omega$  resistor in parallel with this internal 250  $\Omega$  provides an effective input termination of 50  $\Omega$  to the signal source. The circuit shows an ac-coupled input. An internal reference voltage of 2.4 V sets the input CM voltage of the AD9042.

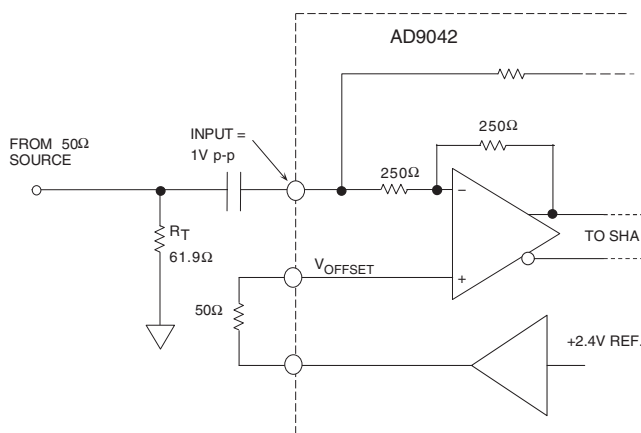


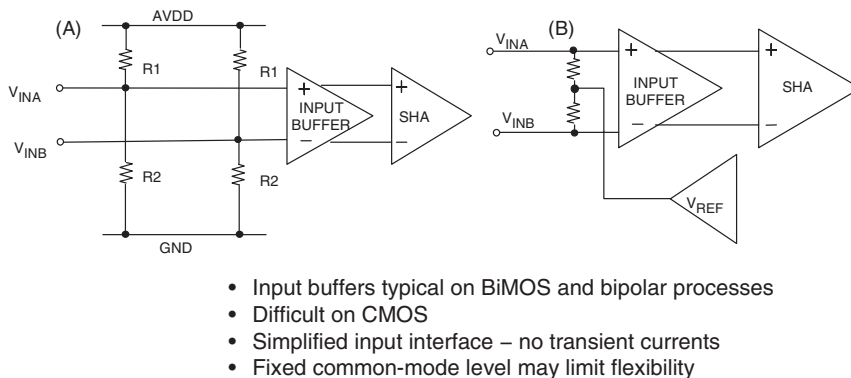
Figure 3-31: AD9042 ADC is designed to be driven directly from 50  $\Omega$  source for best SFDR



The input amplifier precedes the ADC sample-and-hold (SHA), and therefore isolates the input from any transients produced by the conversion process. The gain of the amplifier is set such that the input range of the ADC is 1 V p-p. In the case of a single-ended input structure, the input amplifier serves to convert the single-ended signal to a differential one, which allows fully differential circuit design techniques to be used throughout the remainder of the ADC.

### Driving Buffered Differential Input ADCs

Figure 3-32 below shows two possible input structures for an ADC with buffered differential inputs. The input CM voltage is set with an internal resistor divider network in Figure 3-32A (left), and by a voltage reference in Figure 3-32B (right).



- Input buffers typical on BiMOS and bipolar processes
- Difficult on CMOS
- Simplified input interface – no transient currents
- Fixed common-mode level may limit flexibility

**Figure 3-32: Simplified input circuit of typical buffered ADC with differential inputs**

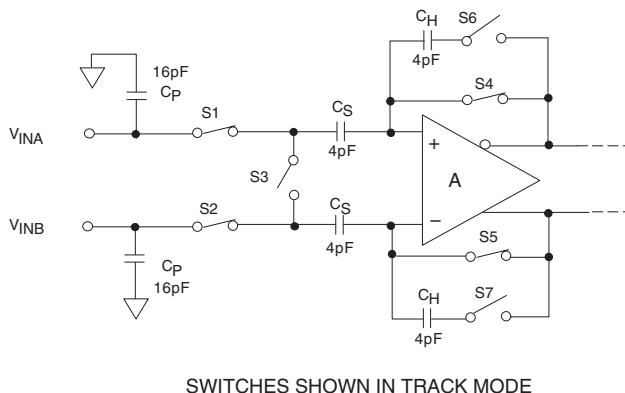
In single supply ADCs, the CM voltage is usually equal to one-half the power supply voltage, but some ADCs may use other values. Although the input buffers provide for a simplified interface, the fixed CM voltage may limit flexibility in some dc coupled applications.

It is worth noting that differential ADC inputs offer several advantages over single-ended ones. First, many signal sources in communications applications are differential (such as the output of a balanced mixer or an RF transformer). Thus, an ADC that accepts differential inputs interfaces easily in such systems. Second, maintaining balanced differential transmission in the signal path and within the ADC itself often minimizes even-order distortion products as well as improving CM noise rejection. Third, (and somewhat more subtly), a differential ADC input swing of say, 2 V p-p requires only 1 V p-p from twin driving sources. On low voltage and single-supply systems, this lower absolute level of drive can often make a real difference in the dual amplifier driver distortion, due to practical headroom limitations.

Given all of these points, it behooves the system engineer to operate a differential-capable ADC in the differential mode for best overall performance. This may be true even if a second amplifier must be added for the complementary drive signal, since dual op amps are only slightly more expensive than singles.

## Driving CMOS ADCs with Switched Capacitor Inputs

CMOS ADCs are quite popular because of their low power and low cost. The equivalent input circuit of a typical CMOS ADC using a differential sample-and-hold is shown in Figure 3-33. While the switches are shown in the *track* mode, note that they open/ close at the sampling frequency. The 16 pF capacitors represent the effective capacitance of switches S1 and S2, plus the stray input capacitance. The  $C_S$  capacitors (4pF) are the sampling capacitors, and the  $C_H$  capacitors are the hold capacitors. Although the input circuit is completely differential, this ADC structure can be driven either single-ended or differentially. Optimum performance, however, is generally obtained using a differential transformer or differential op amp drive.



**Figure 3-33: Simplified input circuit for a typical switched capacitor CMOS sample-and-hold**

In the *track* mode, the differential input voltage is applied to the  $C_S$  capacitors. When the circuit enters the *hold* mode, the voltage across the sampling capacitors is transferred to the  $C_H$  hold capacitors and buffered by the amplifier A (the switches are controlled by the appropriate sampling clock phases). When the SHA returns to the *track* mode, the input source must charge or discharge the voltage stored on  $C_S$  to a new input voltage. This action of charging and discharging  $C_S$ , averaged over a period of time and for a given sampling frequency,  $f_s$ , makes the input impedance appear to have a benign resistive component. However, if this action is analyzed within a sampling period ( $1/f_s$ ), the input impedance is dynamic, and certain input drive source precautions should be observed.

The resistive component to the input impedance can be computed by calculating the average charge that is drawn by  $C_H$  from the input drive source. It can be shown that if  $C_S$  is allowed to fully charge to the input voltage before switches S1 and S2 are opened, the average current into the input is the same as if there were a resistor equal to  $1/(C_S f_s)$  connected between the inputs. Since  $C_S$  is only a few picofarads, this resistive component is typically greater than several k $\Omega$  for an  $f_s = 10$  MSPS.

Over a sampling period, the SHA's input impedance appears as a dynamic load. When the SHA returns to the track mode, the input source should ideally provide the charging current through the  $R_{ON}$  of switches S1 and S2 in an exponential manner. The requirement of exponential charging means that the source impedance should be both low and resistive up to and beyond the sampling frequency.

The output impedance of an op amp can be modeled as a series inductor and resistor. When a capacitive load is switched onto the output of the op amp, the output will momentarily change due to its effective

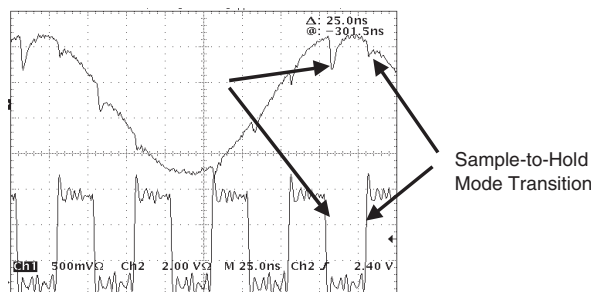
high frequency output impedance. As the output recovers, ringing may occur. To remedy this situation, a series resistor can be inserted between the op amp and the SHA input. The optimum value of this resistor is dependent on several factors including the sampling frequency and the op amp selected, but in most applications, a 25  $\Omega$  to 100  $\Omega$  resistor is optimum.

### Single-Ended ADC Drive Circuits

Although most CMOS ADC inputs are differential, they can be driven single-ended with some ac performance degradation. An important consideration in CMOS ADC applications are the input switching transients previously discussed.

For instance, the input switching transient on one of the inputs of the AD9225 12-bit, 25 MSPS ADC is shown in Figure 3-34. This data was taken driving the ADC with an equivalent 50  $\Omega$  source impedance. During the sample-to-hold transition, the input signal is sampled when  $C_S$  is disconnected from the source. Notice that during the hold-to-sample transition,  $C_S$  is reconnected to the source for recharging. The transients consist of linear, nonlinear, and CM components at the sample rate. In addition to selecting an op amp with sufficient bandwidth and distortion performance, the output should settle to these transients during the sampling interval,  $1/f_s$ . The general circuit shown in Figure 3-35 is typical for this type of single-ended op amp ADC driver application.

- Hold-to-Sample Mode Transition –  $C_S$  Returned to Source for “recharging.” Transient Consists of Linear, Nonlinear, and Common-Mode Components at Sample Rate.
- Sample-to-Hold Mode Transition – Input Signal Sampled when  $C_S$  is disconnected from Source.

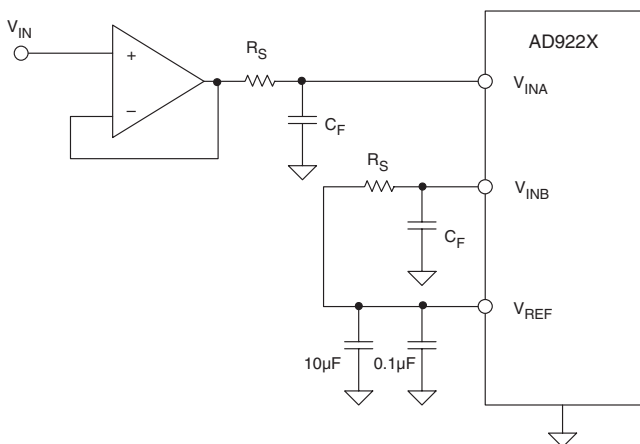


**Figure 3-34: Single-ended input transient response of CMOS switched capacitor SHA (AD9225)**

In this circuit, series resistor  $R_S$  has a dual purpose. Typically chosen in the range of 25  $\Omega$ –100  $\Omega$ , it limits the peak transient current from the driving op amp. Importantly, it also decouples the driver from the ADC input capacitance (and possible phase margin loss).

Another feature of the circuit are the dual networks of  $R_S$  and  $C_F$ . Matching both the dc and ac the source impedance for the ADC’s  $V_{INA}$  and  $V_{INB}$  inputs ensures symmetrical settling of CM transients, for optimum noise and distortion performance. At both inputs, the  $C_F$  shunt capacitor acts as a charge reservoir and steers the CM transients to ground.

In addition to the buffering of transients,  $R_S$  and  $C_F$  also form a low-pass filter for  $V_{IN}$ , which limits the output noise of the drive amplifier into the ADC input  $V_{INA}$ . The exact values for  $R_S$  and  $C_F$  are generally



**Figure 3-35: Optimizing single-ended switched capacitor ADC input drive circuit**

optimized within the circuit, and the recommended values given on the ADC data sheet. The ADC data sheet information should also be consulted for the recommended drive op amp for best performance.

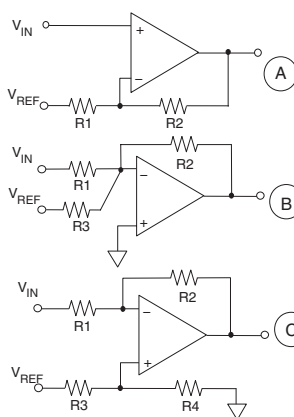
To enable best correlation of performance between environments, an ADC evaluation board should be used (if available). This will ensure confidence when the ADC data sheet circuit performance is duplicated. Analog Devices makes evaluation boards available for many of their ADC and DAC devices (plus, of course, op amps), and general information on them is contained in Chapter 7 of this book.

### Op Amp Gain Setting and Level Shifting in DC-Coupled Applications

In dc-coupled applications, the drive amplifier must provide the required gain and offset voltage, to match the signal to the input voltage range of the ADC. Figure 3-36 summarizes various op amp gain and level-shifting options. The circuit of Figure 3-36A operates in the noninverting mode, and uses a low impedance reference voltage,  $V_{REF}$ , to offset the output. Gain and offset interact according to the equation:

$$V_{OUT} = \left[1 + \left(\frac{R_2}{R_1}\right)\right] \cdot V_{IN} - \left[\left(\frac{R_2}{R_1}\right) \cdot V_{REF}\right] \quad \text{Eq. 3-4}$$

**Figure 3-36: Op amp gain and level shifting circuits**



$$V_{OUT} = \left(1 + \frac{R_2}{R_1}\right) \cdot V_{IN} - \frac{R_2}{R_1} \cdot V_{REF}$$

$$\text{NOISE GAIN} = 1 + \frac{R_2}{R_1}$$

$$V_{OUT} = -\frac{R_2}{R_1} \cdot V_{IN} - \frac{R_2}{R_3} \cdot V_{REF}$$

$$\text{NOISE GAIN} = 1 + \frac{R_2}{R_1 \parallel R_3}$$

$$V_{OUT} = -\frac{R_2}{R_1} \cdot V_{IN} + \left(\frac{R_4}{R_3 + R_4}\right) \left(1 + \frac{R_2}{R_1}\right) \cdot V_{REF}$$

$$\text{NOISE GAIN} = 1 + \frac{R_2}{R_1}$$

The circuit in Figure 3-36B operates in the inverting mode, and the signal gain is independent of the offset. The disadvantage of this circuit is that the addition of R3 increases the noise gain, and hence the sensitivity to the op amp input offset voltage and noise. The input/output equation is given by:

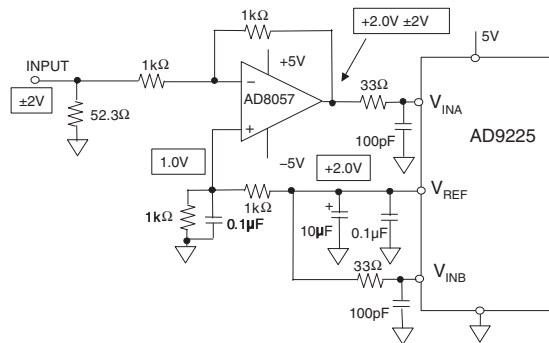
$$V_{OUT} = -(R2/R1) \cdot V_{IN} - (R2/R3) \cdot V_{REF} \quad \text{Eq. 3-5}$$

The circuit in Figure 3-36C also operates in the inverting mode, and the offset voltage  $V_{REF}$  is applied to the noninverting input without noise gain penalty. This circuit is also attractive for single-supply applications ( $V_{REF} > 0$ ). The input/output equation is given by:

$$V_{OUT} = -(R2/R1) \cdot V_{IN} + \left[ \left( R4/(R3 + R4) \right) (1 + (R2/R1)) \right] \cdot V_{REF} \quad \text{Eq. 3-6}$$

Note that the circuit of Figure 3-36A is sensitive to the impedance of  $V_{REF}$ , unlike the counterparts in B and C. This is due to the fact that the signal current flows into/from  $V_{REF}$ , due to  $V_{IN}$  operating the op amp over its CM range. In the other two circuits the CM voltages are fixed, and no signal current flows in  $V_{REF}$ .

A dc-coupled single-ended op amp driver for the AD9225 12-bit, 25 MSPS ADC is shown in Figure 3-37. This circuit interfaces a  $\pm 2$  V input signal to the single-supply ADC, and provides transient current isolation. The ADC input voltage range is 0 V to 4 V, and a dual supply op amp is required, since the ADC minimum input is 0 V.

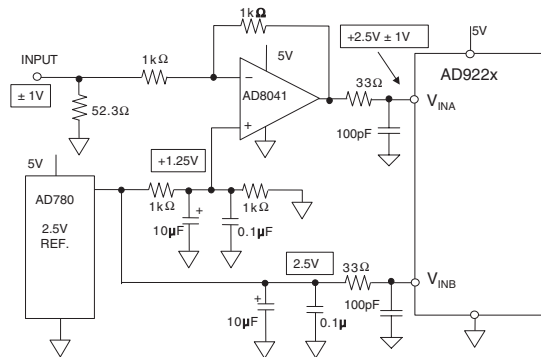


**Figure 3-37: Dc-coupled single-ended level shifter and driver for the AD9225 12-bit, 25 MSPS CMOS ADC**

The noninverting input of the AD8057 is biased at 1 V, which sets the output CM voltage at  $V_{INA}$  to 2 V for a bipolar input signal source. Note that the  $V_{INA}$  and  $V_{INB}$  source impedances are matched for better CM transient cancellation. The 100 pF capacitors act as small charge reservoirs for the input transient currents, and also form low-pass noise filters with the 33  $\Omega$  series resistors.

A similar level shifter and drive circuit is shown in Figure 3-38, operating on a single 5 V supply. In this circuit the bipolar  $\pm 1$  V input signal is interfaced to the input of the ADC whose span is set for 2 V about a +2.5 V CM voltage. The AD8041 rail-to-rail output op amp is used. The 1.25 V input CM voltage for the AD8041 is developed by a voltage divider from the external AD780 2.5 V reference.

Note that single-supply circuits of this type must observe op amp input and output CM voltage restrictions, to prevent clipping and excess distortion.



**Figure 3-38: Dc-coupled single-ended, single-supply ADC driver/level shifter using external reference**

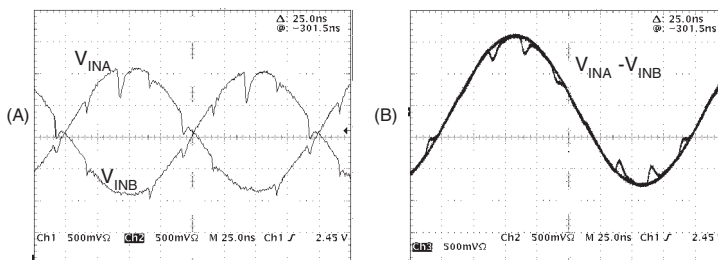
### Drivers for Differential Input ADCs

Most high performance ADCs are now being designed with differential inputs. A fully differential ADC design offers the advantages of good CM rejection, reduction in second-order distortion products, and simplified dc trim algorithms. Although they can be driven single-ended as previously described, a fully differential driver usually optimizes overall performance.

- High common-mode noise rejection
- Flexible input common-mode voltage levels
- Reduced input signal swings helps in low voltage, single-supply applications
- Reduced second-order distortion products
- Simplified dc trim algorithms because of internal matching
- Requires high performance differential driver

**Figure 3-39: Differential input ADCs offer performance advantages**

Waveforms at the two inputs of the AD9225 12-bit, 25 MSPS CMOS ADC are shown in Figure 3-40A, designated as  $V_{INA}$  and  $V_{INB}$ . The balanced source impedance is  $50\ \Omega$ , and the sampling frequency is set for 25 MSPS. The diagram clearly shows the switching transients due to the internal ADC switched capacitor sample-and-hold. Figure 3-40B shows the difference between the two waveforms,  $V_{INA} - V_{INB}$ .

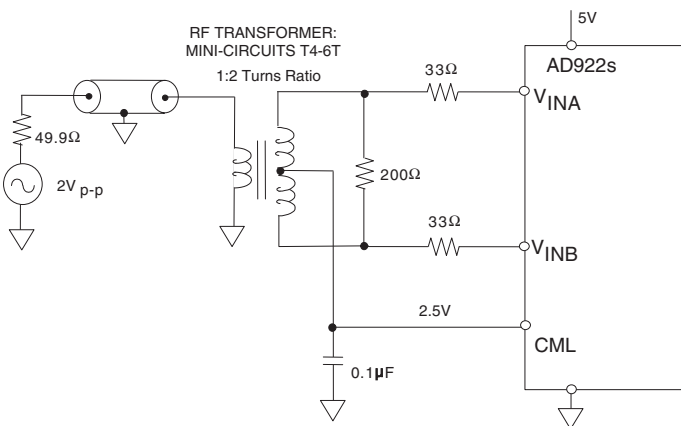


- Differential charge transient is symmetrical around midscale and dominated by linear component
- Common-mode transients cancel with equal source impedance

**Figure 3-40: Differential input transient response of CMOS switched capacitor SHA (AD9225)**

Note that the resulting differential charge transients are symmetrical about midscale, and that there is a distinct linear component to them. This shows the reduction in the CM transients, and also leads to better distortion performance than would be achievable with a single-ended input.

Transformer coupling into a differential input ADC provides excellent CM rejection and low distortion if performance to dc is not required. Figure 3-41 shows a typical circuit. The transformer is a Mini-Circuits RF transformer, model #T4-6T which has an impedance ratio of 4 (turns ratio of 2). The schematic assumes that the signal source has a  $50\ \Omega$  source impedance. The 1:4 impedance ratio requires the  $200\ \Omega$  secondary termination for optimum power transfer and low VSWR. The Mini-Circuits T4-6T has a 1 dB bandwidth



**Figure 3-41: Transformer coupling into AD922x ADC**

from 100 kHz to 100 MHz. The center tap of the transformer provides a convenient means of level shifting the input signal to the optimum CM voltage of the ADC. The AD922x CML (common-mode level) pin is used to provide the +2.5 CM voltage.

Transformers with other turns ratios may also be selected to optimize the performance for a given application. For example, a given input signal source or amplifier may realize an improvement in distortion performance at reduced output power levels and signal swings. Hence, selecting a transformer with a higher impedance ratio (i.e. Mini-Circuits #T16-6T with a 1:16 impedance ratio, turns ratio 1:4) effectively “steps up” the signal level thus reducing the driving requirements of the signal source.

Note the  $33\ \Omega$  series resistors inserted between the transformer secondary and the ADC input. These values were specifically selected to optimize both the SFDR and the SNR performance of the ADC. They also provide isolation from transients at the ADC inputs. Transients currents are approximately equal on the  $V_{\text{INA}}$  and  $V_{\text{INB}}$  inputs, so they are isolated from the primary winding of the transformer by the transformer’s CM rejection.

Transformer coupling using a CM voltage of +2.5 V provides the maximum SFDR when driving the AD922x series. By driving the ADC differentially, even-order harmonics are reduced compared with the single-ended circuit.

## Driving ADCs with Differential Amplifiers

There are many applications where differential input ADCs cannot be driven with transformers because the frequency response must extend to dc. In these cases, op amps can be used to implement the differential drivers. Figure 3-42 shows how the dual AD8058 op amp can be connected to convert a single-ended bipolar signal to a differential one suitable for driving the AD922X family of ADCs. The input range of the ADC is set for a 2 V p-p signal on each input (4 V span), and a CM voltage of +2 V.

The A1 amplifier is configured as a noninverting op amp. The  $1\ \text{k}\Omega$  divider resistors level shift the  $\pm 1\ \text{V}$  input signal to +1 V  $\pm 0.5\ \text{V}$  at the noninverting input of A1. The output of A1 is therefore +2 V  $\pm 1\ \text{V}$ .

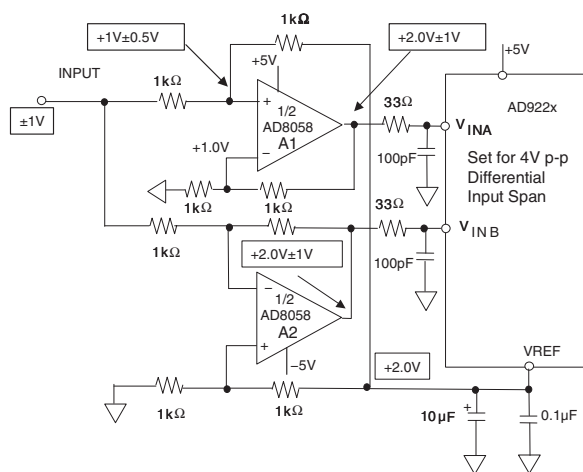


Figure 3-42: Op amp single-ended to differential dc-coupled driver with level shifting.



The A2 op amp inverts the input signal, and the 1 k $\Omega$  divider resistors establish a +1 V CM voltage on its noninverting input. The output of A2 is therefore +2 V  $\pm$ 1 V.

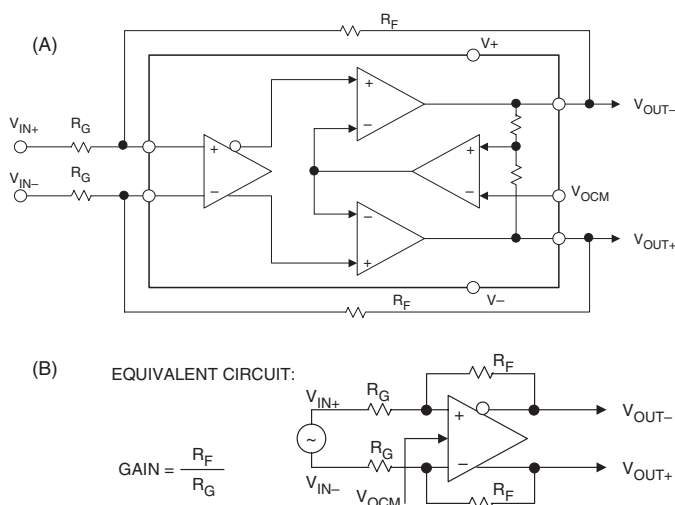
This circuit provides good matching between the two op amps because they are duals on the same die and are both operated at the same noise gain of 2. However, the input voltage noise of the AD8058 is 20 nV/ $\sqrt{\text{Hz}}$ , and this appears as 40 nV/ $\sqrt{\text{Hz}}$  at the output of both A1 and A2 thereby introducing possible SNR degradation in some applications. In the circuit of Figure 3-42, this is mitigated somewhat by the 100 pF input capacitors which not only reduce the input noise but absorb some of the transient currents. It should be noted that because the input CM voltage of A1 can go as low as 0.5 V, dual supplies must be used for the op amps.

A block diagram of the AD813x family of fully differential amplifiers optimized for ADC driving is shown in Figure 3-43 (see References 3-5). Figure 3-43A shows the details of the internal circuit, and Figure 3-43B shows the equivalent circuit. The gain is set by the external  $R_F$  and  $R_G$  resistors, and the CM voltage is set by the voltage on the  $V_{\text{OCM}}$  pin. The internal CM feedback forces the  $V_{\text{OUT}+}$  and  $V_{\text{OUT}-}$  outputs to be balanced, i.e., the signals at the two outputs are always equal in amplitude but 180° out of phase per the equation,

$$V_{\text{OCM}} = (V_{\text{OUT}+} + V_{\text{OUT}-})/2 \quad \text{Eq. 3-7}$$

The circuit can be used with either a differential or a single-ended input, and the voltage gain is equal to the ratio of  $R_F$  to  $R_G$ .

The AD8138 has a 3 dB small-signal bandwidth of 320 MHz ( $G = +1$ ) and is designed to give low harmonic distortion as an ADC driver. The circuit provides excellent output gain and phase matching, and the balanced structure suppresses even-order harmonics.



**Figure 3-43: AD813x differential ADC driver functional diagram and equivalent circuit**

Figure 3-44 shows the AD8138 driving the AD9203 10-bit, 40 MSPS ADC (see Reference 6). This entire circuit operates on a single 3 V supply. A 1 V p-p bipolar single-ended input signal produces a 1 V p-p differential signal at the output of the AD8138, centered around a CM voltage of 1.5 V (mid-supply).

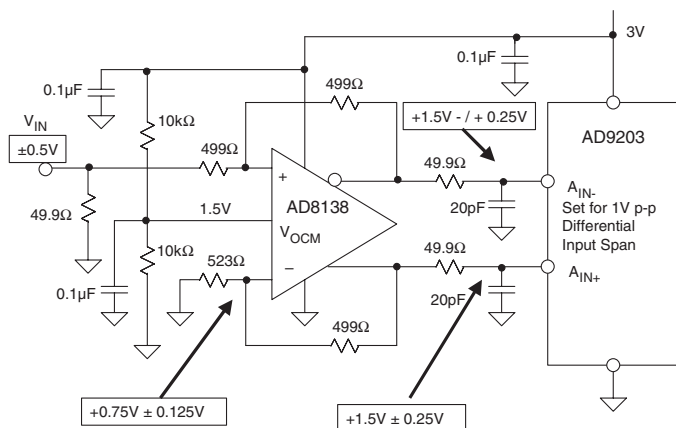


Figure 3-44: AD8138 driving AD9203 10-bit, 40 MSPS ADC

Each of the differential inputs of the AD8138 swing between +0.625 V and +0.875 V, and each output swings between 1.25 V and 1.75 V. These voltages fall within the allowable input and output CM voltage range of the AD8138 operating on a single 3 V supply.

The circuit as shown operates on a 1 V p-p single-ended bipolar input signal, and the input span of the AD9203 ADC is set for 1 V p-p differential. If the signal input amplitude is increased to 2 V p-p, the span of the AD9203 must be set for 2 V p-p differential. Under these conditions, each of the AD8138 inputs must swing between 0.5 V and 1 V, and each of the outputs between 1 V and 2 V.

As shown in Figure 3-45, increasing the amplitude in this manner offers a slight improvement in low frequency SINAD due to the improvement in low frequency SNR.

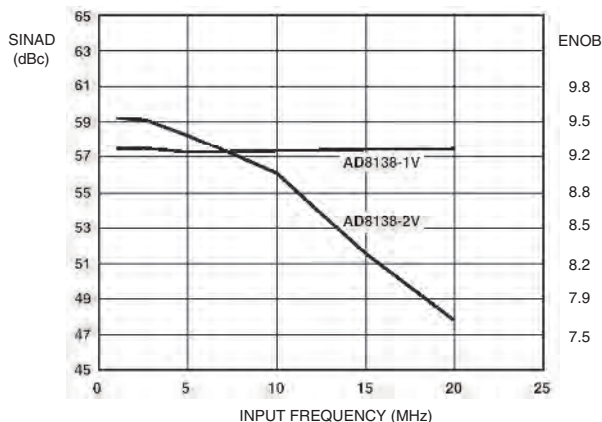


Figure 3-45: SINAD and ENOB for AD9203 12-bit, 40 MSPS ADC driven by AD8138 differential amplifier

At the same time however, a degradation occurs in the high frequency SINAD because of the larger distortion due to the larger signal swings.

## Overvoltage Considerations

The input structures of most high performance ADCs are sensitive to overvoltage conditions because of the small geometry devices used in the designs. Although ADC inputs generally have ESD protection diodes connected from the analog input to each supply rail, these diodes are not designed to handle the large currents that can be generated from typical op amp drivers. Two good rules of thumb are to (1) limit the analog input voltage to no more than 0.3 V above or below the positive and negative supply voltages, respectively, and (2) limit the analog input current to 5 mA maximum in overvoltage conditions.

Several typical configurations for the drive amp/ADC interface are shown in Figure 3-46. In Figure 3-46A, the ADC requires no additional input protection because both the op amp and the ADC are driven directly from the same supply voltages. While the  $R_S$  resistor is not required for overvoltage protection, it does serve to isolate the capacitive input of the ADC from the output of the op amp.

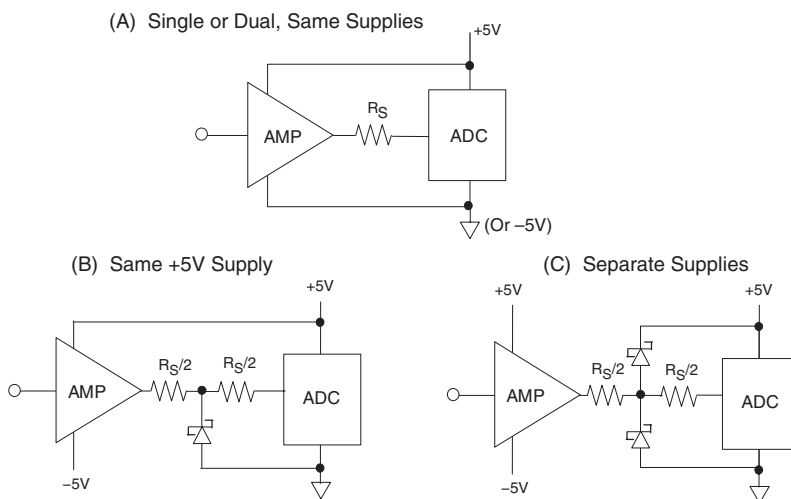


Figure 3-46: ADC input overvoltage protection circuits

Figure 3-46B shows a dual supply op amp driving a single supply ADC, with the 5 V supply is shared between the two devices. The diode protects the input of the ADC in case the output of the op amp is driven below ground. A Schottky diode is used because of its low forward voltage drop and its low capacitance. The  $R_S$  resistor is split into two equal resistors, and they are chosen to limit the ADC input fault current to 5 mA maximum. Note that the  $R_S$  resistor in conjunction with the ADC input capacitance forms a low-pass filter. If  $R_S$  is made too large, the input bandwidth may be restricted.

Figure 3-46C shows the condition where the op amp and the ADC are driven from separate supplies. Two Schottky diodes are required to protect the ADC under all power supply and signal conditions. As in 3-46A, the  $R_S/2$  resistors limit ADC fault current.

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## **References: Driving ADC Inputs**

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